STD-HLS34-V6.2E

STEP TECHNICA CO.,LTD.

# Hi-speed Link System

# Satellite IC

# MKY34

# User's Manual

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# Preface

This manual describes the MKY34, or a kind of satellite IC in the Hi-speed Link System.
Be sure to read ***"Hi-speed Link System Introduction Guide"*** before understanding this manual and the MKY34.
In this manual, the Hi-speed Link System is abbreviated as "HLS".

● **Target Readers**

This manual is for:
- Those who first build an HLS
- Those who first use StepTechnica's various ICs to build an HLS

● **Prerequisites**

This manual assumes that you are familiar with:
- Network technology
- Semiconductor products (especially microcontrollers and memory)

● **Related Manuals**

- Hi-speed Link System Introduction Guide
- Hi-speed Link System Technical Guide

**[Caution]**

- **To users with *"Hi-speed Link System User's Manual"* up to "Fourth Edition" released before March, 2001**
  Some terms in this manual have been changed to conform to International Standards.

■ This manual has been prepared based on Standard English™ meeting the requirements of the International Organization for Standardization (ISO) and the American National Standards Institute (ANSI). This English manual is consistent with the Japanese document **"STD-HLS34-V6.2J"**.

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This chapter describes the outline of the MKY34 in the Hi-speed Link System (HLS).

# Chapter 1 Outline of MKY34

This chapter describes the outline of the MKY34 in the Hi-speed Link System (HLS).

## 1.1 Role of MKY34

MKY34 is a kind of satellite IC that constitutes the HLS. Be sure to read the ***"Hi-speed Link System Introduction Guide"*** before understanding the MKY34 and this manual.
The MKY34 must be assigned individual satellite addresses (SAs).

The MKY34 returns a response packet (RP) in response to a command packet (CP), which matches a SA, from the center IC. This causes the status of the input pin (Di) of the MKY34 to be copied directly to the Di area of memory in the center IC. The CP issued from the center IC is embedded with one data item arranged in the Do area of memory in the center IC.

The MKY34 outputs data in the CP from the output pin (Do) of the MKY34 each time a CP matching a SA is input. The center IC periodically transmits and receives a CP to continue scanning the satellite IC. This series of continuous operation links the status of the input pin (Di) of the MKY34 with data in the Di area of memory in the center IC, and data arranged in the Do area of memory in the center IC with the status of the output pin (Do) of the MKY34. The Di and Do areas of memory in the center IC are arranged corresponding to each SA that must be set to the MKY34 (Fig. 1.1).
The MKY34 has some expanded functions in addition to input pin (Di) and output pin (Do) for embedding in various user systems.

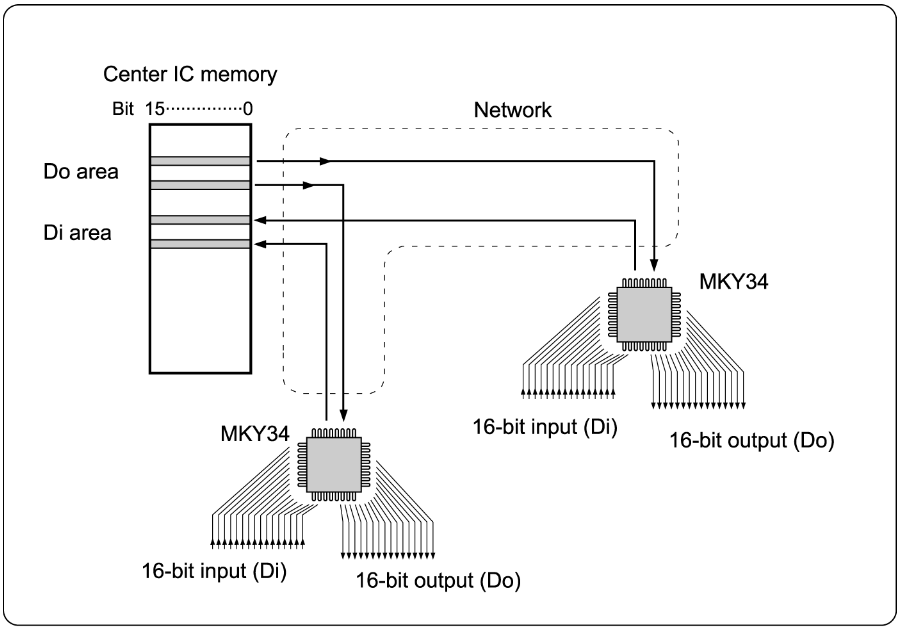


Fig. 1.1 Role of MKY34

## 1.2 Procedure for Operating MKY34

The MKY34 is a passive IC and it is operated by remote control from center ICs. The user system program (for access to center ICs) to use the MKY34 is very simple.

(1) The user system program just writes data to memory in the center IC when it wants to change the status of the output pin (Do) of the MKY34. For example, when a relay is connected to the output pin (Do), the user system program simply writes data to memory in the center IC only when it wants to turn the relay on or off.

(2) The user system program simply reads memory in the center IC when it wants to obtain the status of the input pin (Di) of the MKY34. For example, when a sensor is connected to the input pin (Di), the user system program can obtain the status of the sensor by reading memory in the center IC.

(3) The user system program can operate the MKY34's expanded functions simply by handling a command in memory in the center IC.

## 1.3 MKY34 Response Time

In the HLS where a center IC continues to scan, constancy of response time and real-timeness are assured. The time required to link data in memory in the center IC with the states of the input pin (Di) and output pin (Do) of the MKY34 essentially matches the scan time of the HLS, which is very short.

For example, in a user system that must detect the exact position of each box on a belt conveyor, if four MKY34s are connected to the center IC and position detection sensors are connected to the input pins (Di) of all MKY34s, the status of 64 sensors (16 sensors × 4 MKY34s) is stored to memory in the center IC with a scan time interval of 60.7 μs (12 Mbps: full duplex), keeping data up-to-date. This speed remains unchanged even if the farthest MKY34 is 100-m distant. Even if the position detection sensors are placed at every 5 cm, they can detect the position of every box on the belt conveyor without mistakes even when the conveyor runs at 823 m/s (>2900 km/h).

Reference

For details of the scan time, refer to ***"Scan Time"*** in ***"User's Manual"*** for the center IC connecting the MKY34.

## 1.4 Features of MKY34

This section describes the basic and the expanded functions of the MKY34.

### 1.4.1 Features of Basic Functions of MKY34 as Satellite IC in HLS

(1) Has 16 input pins (Di) and 16 output pins (Do)
(2) Supports baud rates of 12, 6, and 3 Mbps
(3) Supports full- and half-duplex modes
(4) Has six pins to set satellite addresses (SA) for any one of 63 terminals at 01H to 3FH
(5) Operates on 5.0-V single power supply and available in 0.8 mm pitch, 84 pins, QFP

### 1.4.2 Expanded Functions

(1) Has CLR pin that sets output pins (Do) Low
(2) Has strobe output pins that indicate timing to update output pins (Do) and receive input pins (Di)
The user can also design peripheral circuits based on each update timing
(3) Can set handshake to ensure link with center IC
(4) Can connect satellite ICs directly by cascade connection
(5) Has 6-channel 16-bit binary up-counter
The user can use a digital filter to prevent miscounting
(6) Has 16-bit Serial IDentification Register (SIDR)
(7) Can backup 6-channel 16-bit binary counter and SIDR values by using battery

# Chapter 2 MKY34 Hardware

This chapter describes the MKY34 hardware, such as pin assignment, pin functions, and I/O circuit types.

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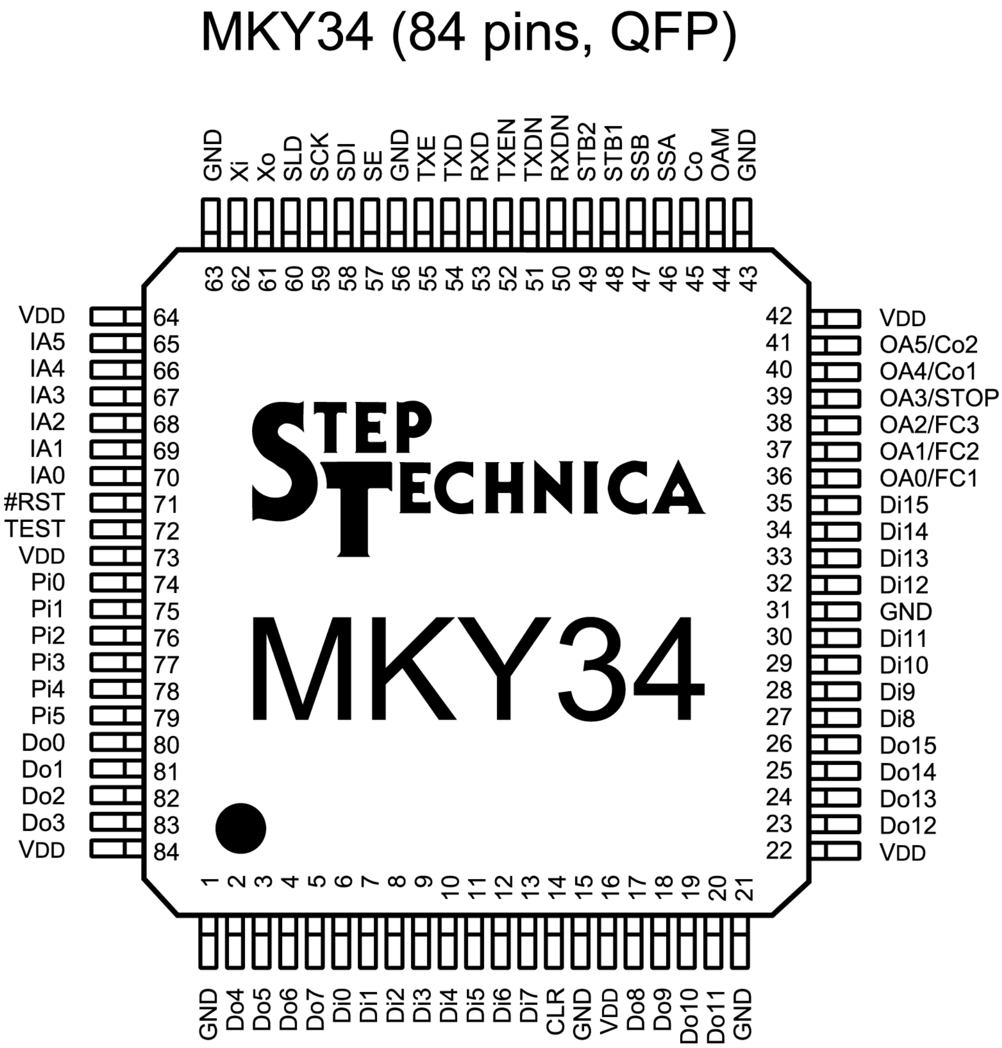
Figure 2.1 shows the MKY34 pin assignment.




Note: Pins prefixed with # are negative logic (active Low).

Fig. 2.1 MKY34 Pin Assignment

Table 2-1 lists the pin functions of the MKY34.

**Table 2-1 Pin Functions of MKY34**

| Pin name | Pin No. | Logic | I/O | Function |
|---|---|---|---|---|
| Do0 to Do15 | 80 to 83<br>2 to 5<br>17 to 20<br>23 to 26 | Positive | O | 16-bit general-purpose output pins |
| Di0 to Di15 | 6 to 13<br>27 to 30<br>32 to 35 | Positive | I | 16-bit general-purpose input pins |
| CLR | 14 | Positive | I | Input pin to forcibly set all output pins Do0 to Do15 Low<br>Usually, keep this pin Low. |
| OA0 to OA5 | 36 to 41 | Positive | O | Pins to which positive-logic hexadecimal values at which "1" added to set values input to IA0 to IA5 pins output when OAM pin High<br>Connect these pins to the IA0 to IA5 pins of the subsequent satellite IC when cascade-connecting satellite ICs. The OA5 pin is MSB. |
| FC1 | 36* | Positive | I | Pin to input clock for filtering signals input to Pi0 and Pi1 pins when OAM pin Low<br>Fix this pin at High or Low when the filter clock is not input. |
| FC2 | 37* | Positive | I | Pin to input clock for filtering signals input to Pi2 and Pi3 pins when OAM pin Low<br>Fix this pin at High or Low when the filter clock is not input. |
| FC3 | 38* | Positive | I | Pin to input clock for filtering signals input to Pi4 and Pi5 pins when OAM pin Low<br>Fix this pin at High or Low when the filter clock is not input. |
| STOP | 39* | Positive | I | Input pin to put MKY34 in battery backup mode when OAM pin Low<br>Usually, fix this pin at Low.<br>Input a High level for the battery backup of the MKY34. When the MKY34 is placed in battery backup mode, all output pins except the Xo pin enter the high impedance state. |
| Co1 | 40* | Positive | O | Pin to output a driving clock frequency divided by 32768 when OAM Low<br>(Example: Xi: 24 MHz $\rightarrow$ Co1: $\approx$732 Hz) |
| Co2 | 41* | Positive | O | Pin to output a driving clock frequency divided by 262144 when OAM pin Low<br>(Example: Xi: 24 MHz $\rightarrow$ Co2: $\approx$91 Hz) |
| OAM | 44 | Positive | I | Input pin to select functions of pins 36 to 41<br>When using the MKY34 battery backup function and the function for filtering the Pi input, set this pin Low<br>Set this pin High at all other times. |
| Co | 45 | Positive | O | Pin to output a driving clock |
| SSA | 46 | Positive | I | Input a High or Low level for selection of strobe signal functions to this pin. |

(Continue)

**Table 2-1 Pin Functions of MKY34**

(Continued)

| Pin name | Pin No. | Logic | I/O | Function |
|---|---|---|---|---|
| SSB | 47 | Positive | I | Input a High or Low level for selection of strobe signal functions to this pin. |
| STB1 | 48 | Positive | O | Output pin that outputs High-level pulse of strobe signals indicating timing to update state of general-purpose output pins Do0 to Do15 when command packet is input correctly from center IC |
| STB2 | 49 | Positive | O | Output pin that outputs High-level pulse of strobe signals indicating timing to read state of general-purpose input pins Di0 to Di15 |
| RXDN | 50 | Positive | O | Output pin that outputs signal input to RXD pin<br>Connect this pin to the RXD pin of the subsequent satellite IC when cascade-connecting satellite ICs. |
| TXDN | 51 | Positive | I | Connect this pin to the TXD pin of the subsequent satellite IC when cascade-connecting satellite ICs.<br>Be sure to fix this pin at Low when neither cascade-connecting satellite ICs nor using this pin function. |
| TXEN | 52 | Positive | I | Connect this pin to the TXE pin of the subsequent satellite IC when cascade-connecting satellite ICs.<br>Be sure to fix this pin at Low when neither cascade-connecting satellite ICs nor using this pin function. |
| RXD | 53 | Positive | I | Input pin that inputs command packet from center IC<br>Connect this pin to the output pin of a receiver. |
| TXD | 54 | Positive | O | Pin that outputs response packet to center IC<br>Connect this pin to the drive input pin of a driver. |
| TXE | 55 | Positive | O | Output pin that goes High while outputting response packet to center IC<br>Connect this pin to the enable input pin of a driver. |
| SE | 57 | Positive | O | Output pin for serial ID send function<br>This pin goes High when the serial ID send function is enabled to receive serial input. |
| SDI | 58 | Positive | I | Serial ID input pin for serial ID send function<br>Fix this pin at Low when not using the serial ID send function. |
| SCK | 59 | Positive | I | Clock input pin for serial ID send function<br>Fix this pin at Low when not using the serial ID send function. |
| SLD | 60 | Positive | I | Input pin for serial ID send function to input signal indicating completion of serial ID input<br>Fix this pin at Low when not using the serial ID send function. |
| Xo | 61 | Positive | O | Pin for oscillator connection |
| Xi | 62 | Positive | I | Pin for connection of oscillator or generated clock |
| IA0 to IA5 | 70 to 65 | Positive | I | Input pins to assign satellite addresses<br>Set the positive-logic hexadecimal values "1 to 63 (01H to 3FH)" assuming a High level to be "1". A5 is MSB. |

(Continue)

**Table 2-1 Pin Functions of MKY34**

(Continued)

| Pin name | Pin No. | Logic | I/O | Function |
|---|---|---|---|---|
| #RST | 71 | Negative | I | MKY34 Hardware reset input pin<br>Keep this pin Low for 10 or more clocks of the Xi pin frequency right after power-on or when resetting hardware intentionally. |
| TEST | 72 | Positive | I | Be sure to connect this pin to GND (manufacturer test pin) |
| Pi0 to Pi5 | 74 to 79 | Positive | I | Input pins for general-purpose 6-channel counter<br>Fix the inputs of unused counters at High or Low. |
| VDD | 16, 22<br>42, 64<br>73, 84 | --- | --- | Power pin connected to 5.0 V |
| GND | 1, 15<br>21, 31<br>43, 56<br>63 | --- | --- | Power pin connected to 0 V |

Note: Pins prefixed with # are negative logic (active Low).

The pins with numbers suffixed by an asterisk (*) are to be selected when the OAM pin is Low.

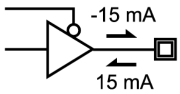
Table 2-2 and Figure 2.2 shows the electrical ratings of the MKY34 pins.

**Table 2-2 Electrical Ratings of MKY34**

(#: Negative logic)

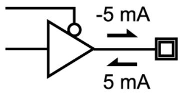
| No | I/O | Name | Type | No | I/O | Name | Type | No | I/O | Name | Type | No | I/O | Name | Type |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | -- | GND | -- | 22 | -- | VDD | -- | 43 | -- | GND | -- | 64 | -- | VDD | -- |
| 2 | O | Do4 | A | 23 | O | Do12 | A | 44 | I | OAM | D | 65 | I | IA5 | E |
| 3 | O | Do5 | A | 24 | O | Do13 | A | 45 | O | Co | A | 66 | I | IA4 | E |
| 4 | O | Do6 | A | 25 | O | Do14 | A | 46 | I | SSA | D | 67 | I | IA3 | E |
| 5 | O | Do7 | A | 26 | O | Do15 | A | 47 | I | SSB | D | 68 | I | IA2 | E |
| 6 | I | Di0 | D | 27 | I | Di8 | D | 48 | O | STB1 | B | 69 | I | IA1 | E |
| 7 | I | Di1 | D | 28 | I | Di9 | D | 49 | O | STB2 | B | 70 | I | IA0 | E |
| 8 | I | Di2 | D | 29 | I | Di10 | D | 50 | O | RXDN | A | 71 | I | #RST | D |
| 9 | I | Di3 | D | 30 | I | Di11 | D | 51 | I | TXDN | D | 72 | I | TEST | D |
| 10 | I | Di4 | D | 31 | -- | GND | -- | 52 | I | TXEN | D | 73 | -- | VDD | -- |
| 11 | I | Di5 | D | 32 | I | Di12 | D | 53 | I | RXD | D | 74 | I | Pi0 | D |
| 12 | I | Di6 | D | 33 | I | Di13 | D | 54 | O | TXD | A | 75 | I | Pi1 | D |
| 13 | I | Di7 | D | 34 | I | Di14 | D | 55 | O | TXE | A | 76 | I | Pi2 | D |
| 14 | I | CLR | D | 35 | I | Di15 | D | 56 | -- | GND | -- | 77 | I | Pi3 | D |
| 15 | -- | GND | -- | 36 | O/I | OA0/FC1 | F | 57 | O | SE | B | 78 | I | Pi4 | D |
| 16 | -- | VDD | -- | 37 | O/I | OA1/FC2 | F | 58 | I | SDI | D | 79 | I | Pi5 | D |
| 17 | O | Do8 | A | 38 | O/I | OA2/FC3 | F | 59 | I | SCK | D | 80 | O | Do0 | A |
| 18 | O | Do9 | A | 39 | O/I | OA3/STOP | F | 60 | I | SLD | D | 81 | O | Do1 | A |
| 19 | O | Do10 | A | 40 | O | OA4/Co1 | C | 61 | O | Xo | -- | 82 | O | Do2 | A |
| 20 | O | Do11 | A | 41 | O | OA5/Co2 | C | 62 | I | Xi | -- | 83 | O | Do3 | A |
| 21 | -- | GND | -- | 42 | -- | VDD | -- | 63 | -- | GND | -- | 84 | -- | VDD | -- |

**Type-A** CMOS level output (With high-impedance control)



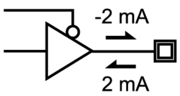

| | | |
|---|---|---|
| $V_{OH}$ min | 4.4 | V |
| V max | 0.4 | V |
| $I_{OH}$ max | -15.0 | mA |
| $I_{OL}$ max | 15.0 | mA |
| $I_Z$ max | ±10 | µA |

**Type-B** CMOS level output (With high-impedance control)



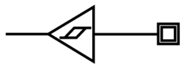

| | | |
|---|---|---|
| $V_{OH}$ min | 4.4 | V |
| $V_{OL}$ max | 0.4 | V |
| $I_{OH}$ max | -5.0 | mA |
| $I_{OL}$ max | 5.0 | mA |
| $I_Z$ max | ±10 | µA |

**Type-C** CMOS level output (With high-impedance control)



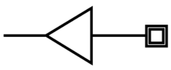

| | | |
|---|---|---|
| $V_{OH}$ min | 4.4 | V |
| $V_{OL}$ max | 0.4 | V |
| $I_{OH}$ max | -2.0 | mA |
| $I_{OL}$ max | 2.0 | mA |
| $I_Z$ max | ±10 | µA |

**Type-D** CMOS level input (Schmitt trigger)



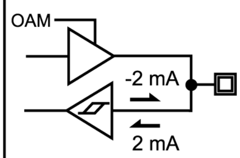
| | | |
|---|---|---|
| Vt+ max | 3.5 | V |
| typ | 2.9 | V |
| Vt- typ | 2.1 | V |
| min | 1.0 | V |
| ΔVt min | 0.8 | V |
| $I_{IH}$ max | 10 | µA |
| $I_{IL}$ max | -10 | µA |

**Type-E** CMOS level input



| | | |
|---|---|---|
| $V_{IH}$ min | 3.5 | V |
| $V_{IL}$ max | 1.5 | V |
| $I_{IH}$ max | 10 | µA |
| $I_{IL}$ max | -10 | µA |

**Type-F** CMOS level input/output (Schmitt trigger)




| | | |
|---|---|---|
| $V_{OH}$ min | 4.4 | V |
| $V_{OL}$ max | 0.4 | V |
| Vt+ max | 3.5 | V |
| typ | 2.9 | V |
| Vt- typ | 2.1 | V |
| min | 1.0 | V |
| ΔVt min | 0.8 | V |
| $I_{IH}$ max | 10 | µA |
| $I_{IL}$ max | -10 | µA |
| $I_{OH}$ max | -2.0 | mA |
| $I_{OL}$ max | 2.0 | mA |
| $I_Z$ max | ±10 | µA |

Fig. 2.2 Pin Electrical Characteristics in I/O Circuit Types of MKY34

# Chapter 3 Connecting Basic Functions of MKY34

This chapter describes the pin functions and connections required to operate the basic functions of the MKY34.

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## 3.1 Driving Clock

This section describes the MKY34 driving clock.

### 3.1.1 Self-generation of Driving Clock

The MKY34 can be connected to an oscillator to self-generate a driving clock. In this case, connect the oscillator to the Xi pin (pin 62) and Xo pin (pin 61). The frequency of driving clock to be generated must be four times greater than the baud rate. For example, if the baud rate is 6 Mbps, the frequency of the driving clock is 24 MHz. If the driving clock is generated correctly, the user can find that the Co (Clock out) pin (pin 45) outputs the clock. This clock is output from the Co pin while the hardware reset is activated, so it is usable for cascade connection described later in ***"4.2 Cascade Connection"***.
Place the oscillator and auxiliary component to be connected to the Xi and Xo pins near the MKY34. The allowable oscillating frequency accuracy is within ±5% for a frequency of four times the baud rate. Supported oscillators include crystal and ceramic types. Select an appropriate value for the additional capacitance depending on the oscillator types and manufacturers (Fig. 3.1).

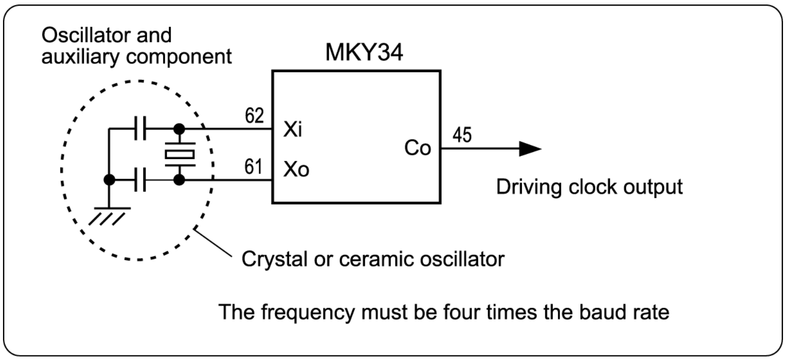



Fig. 3.1 Connecting Oscillator

**Caution**

(1) The MKY34 oscillation frequency ranges from 4 MHz to 30 MHz. If the driving clock frequency outside this range is required, use the generated clock described in ***"3.1.2 Supplying Generated Driving Clock"***.
(2) Some oscillator types may need to be inserted a dumping resistor (DR) between the Xo and oscillator.
(3) The allowable oscillating frequency accuracy is within ±5% for a frequency four times the baud rate. If the frequency accuracy is low, the allowable length of the network cable to the center IC may be short. To prevent this, StepTechnica recommends a crystal oscillator be used to maintain the accuracy within ±1%.
(4) To recognize the oscillating state and measure oscillating frequencies, use the Co pin.

**Reference**

StepTechnica provides some technical information, such as an appropriate capacitance for the oscillator, how to stabilize oscillation, etc. For more information, visit our Web site at **www.steptechnica.com/**

### 3.1.2 Supplying Generated Driving Clock

An oscillator-generated external clock can be supplied directly to the MKY34 and used as the driving clock. To supply the external clock directly to the MKY34, use the Xi pin (pin 62) and leave Xo pin (pin 61) open. The specifications for direct supplying the external clock are as follows:

(1) The upper frequency is 50 MHz and a lower frequency is not provided.
(2) $V_{IH}$ = min. 3.5 V, $V_{IL}$ = max. 1.5 V
(3) Clock with a signal rise and fall times of 20 ns or less
(4) Clock with a minimum High-level or Low-level time of 5 ns or more
(5) Clock with jitter component of:
   - Within 250 ps when input frequency is 25 MHz or more
   - Within 500 ps when input frequency is less than 25 MHz
(6) Frequency accuracy of 1000 ppm (±0.1%) or better

**Reference** For a commonly-used oscillator, there is no problem with clock output by the values above in (2) to (6).

Table 3-1 shows the correspondence between the driving clock and baud rate.

**Table 3-1 Correspondence between Driving Clock and Baud Rate**

| Driving clock | Baud rate | Remarks |
|---|---|---|
| 48 MHz | 12 Mbps | The operating clock cannot be self-generated |
| 24 MHz | 6 Mbps | --------- |
| 12 MHz | 3 Mbps | --------- |

## 3.2 Hardware Reset

When a Low level is input to the #RST (ReSeT) pin (pin 71), the MKY34 is hardware-reset. If a period in which the Low-level signal has been input is less than "one clock", the signal is ignored to prevent malfunction. To reset the MKY34 completely, the #RST pin must be kept Low for "10 or more clock" while supplying a driving clock. The #RST pin is connected to an internal Schmitt-type input buffer, so a constant-rise-time circuit can be connected directly at power-on (Fig. 3.2).

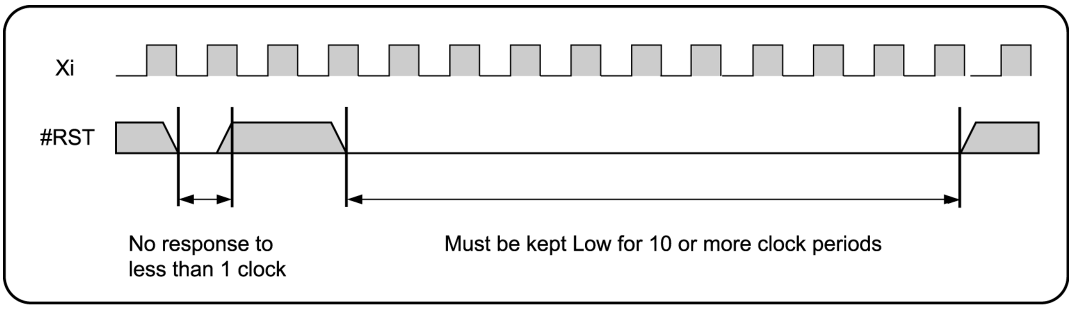



Fig. 3.2 Hardware Reset

**Caution** Design the circuit so that a hardware reset is surely activated immediately after MKY34 power-on.

## 3.3 Setting Satellite Addresses

The MKY34 has six satellite address (SA) setting pins (IA0 to IA5: Input Addresses 0 to 5). Individual satellite addresses (SA) must be assigned to each satellite IC when using the HLS. To set the SA values to the MKY34, use hexadecimal numbers from 01H to 3FH (addresses 1 to 63) assuming a High level is input to IA0 to IA5 (pins 64 to 70) as “1” and a Low level is input as “0”. The most significant bit is IA5 (pin 65). These SA settings correspond to the memory addresses in each area in the center IC.

- **Example 1: The state of the input pin (Di) of the MKY34 at SA = 1 (01H) is stored at address 02H in the Di area of memory in the center IC.**
- **Example 2: The state of the input pin (Di) of the MKY34 at SA = 63 (3FH) is stored at address 7EH in the Di area of memory in the center IC.**
- **Example 3: The data at memory address 9CH in the Do area in the center IC is output to the output pin (Do) of the MKY34 at SA = 14 (0EH).**

**Reference**

There are no limitations on physical network arrangement, such as setting the SA values in the order in which they are closer to the center IC. If the center IC has two input pins (RXD1 and RXD2), there are no rules, such as which pin (network) the MKY34 in which specific SA values are set is connected to.

**Caution**

The different SA values must be set to all satellite ICs connected to one center IC. The SA value cannot be set to 00H. Even if the SA value of 00H is set to a satellite IC by mistake, the system is not adversely affected but the satellite IC is not scanned by the center IC.

## 3.4 Connecting Network Interface

The network interface (network I/F) pins of the MKY34 consist of RXD (pin 53), TXE (pin 55), and TXD (pin 54).

### 3.4.1 Details of RXD, TXE, and TXD Pins

In the MKY34, the RXD pin inputs a command packet (CP) from the center IC. Connect the TRX (driver/receiver components) in the network so that a serial pattern signal for the command packet (CP) transmitted from the center IC will be input to the RXD pin.

If the address of the input CP matches the SA set by IA0 to IA5, the MKY34 immediately returns a response packet (RP) to the center IC. The TXE pin goes High while the MKY34 sends the RP. When the TXE pin goes High, design the TRX so that the enable pin of the TRX driver is activated, thereby enabling the serial pattern signal for the RP output from the TXD pin to be transmitted to the network.
When the hardware reset is activated, the TXE and TXD pins keep the last levels. These pins always go Low whenever the hardware reset is canceled.

Reference

When the HLS operates in half-duplex mode, the signal output from the TXD pin of the MKY34 may be input directly to the RXD pin while the MKY34 is returning the RP. The MKY34 is designed not to input data when the TXE pin is High, so there is no problem.

### 3.4.2 Recommended Network Connection

Figure 3.3 shows the recommended network connection.  The TRX (driver/receiver components) consists of an RS485-based driver/receiver (LSI driven at 5.0 V) and pulse transformer.  Recommended network cables include Ethernet LAN network cables (10BASE-T, Category 3 or higher) and shielded network cables.  When operating the HLS, full-duplex mode requires two twisted-pair cables, and half-duplex requires one twisted-pair cable (Fig. 3.3).

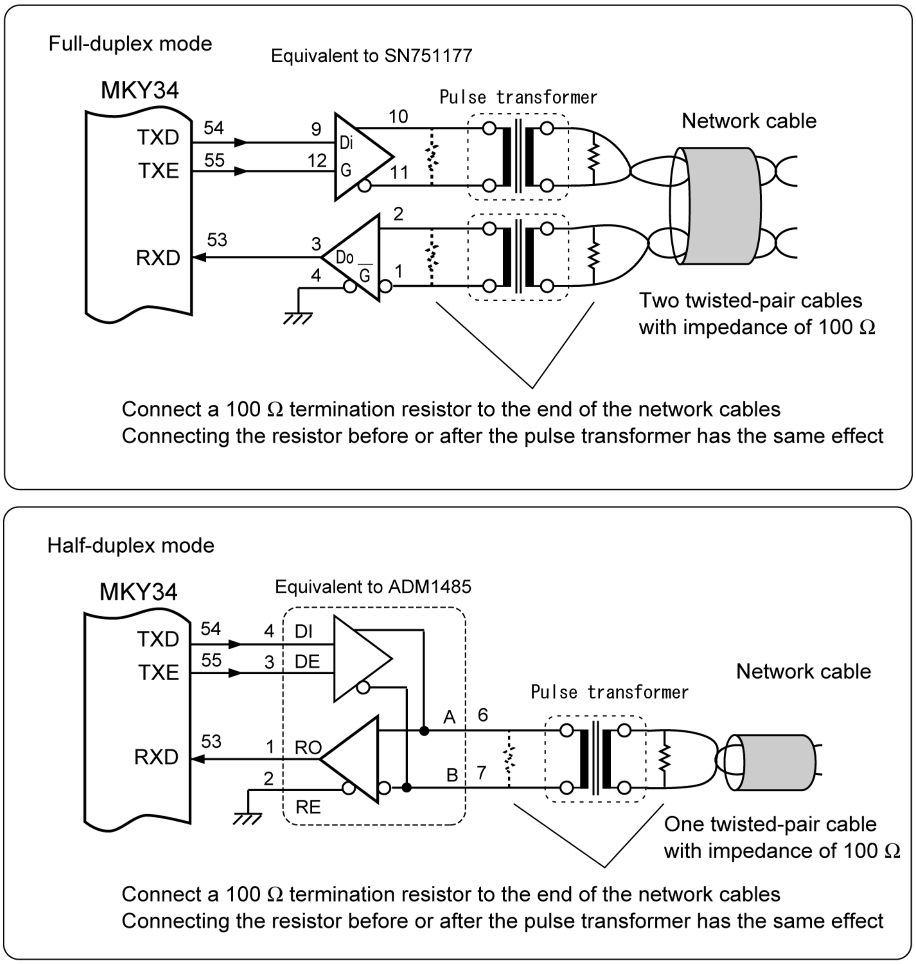



Fig. 3.3   Recommended Network Connection

**Reference**

The High-level signal output from the TXE pin (pin 55) of the network interface can be used to detect that the center IC is scanning.  It can also be used to check the operation of the user system using the HLS and measure the response speed.

Background information to help build network cables is described in ***"Hi-speed Link System Technical Guide"***.  For more information about how to select components or to get recommended components, visit our Web site at **www.steptechnica.com/**

## 3.5 16 Input Pins (Di)

The MKY34 has 16 input pins (Di0 to Di15). The state of the input pins is copied directly to the memory address corresponding to the SA in the Di area in the center IC. Di0 (pin 6) corresponds to data bit 0 and Di15 (pin 35) corresponds to data bit 15, which link as 16-bit word data to memory in the center IC. The Di0 to Di15 pins have Schmitt input buffers and can be connected directly to time-constant circuits for chattering prevention.

**Caution**

If any I/O input pins of the Di0 to Di15 are unused in the user system, they cannot be left open. Fix them at High or Low (pins to be used for future should be connected to a pull-up or pull-down resistor). When a command in the command packet (CP) issued from the center IC is not "0" or "8" (basic function specified) and the user system program performs the operation using the expanded functions of the MKY34 described later, data at the Di0 to Di15 pins is not sent to the Di area.
When a command in the CP issued from the center IC is "0" or "8" and High level is input to the CLR pin at the right time to get states of the input pins (Di0 to Di15), "FFFFH" data is sent to the Di area.

## 3.6 16 Output Pins (Do)

The MKY34 has 16 output pins (Do0 to Do15). When the MKY34 inputs the CP correctly which contains one piece of the data in the Do area in the center IC (memory) issued from the center IC, and when the address of the CP matches the SA set by IA0 to IA5, the MKY34 outputs (updates) the data contained in the CP to the output pins (Do0 to Do15) of the MKY34. The data output to the I/O output pins is kept until next updated. The Do0 pin (80) corresponds to bit 0 of the 16-bit word data in the Do area in the center IC (memory) and Do15 (pin 26) to bit 15.

When a hardware reset is activated, the output pins (Do0 to Do15) keep the last levels. These pins always go Low whenever the hardware reset is canceled.
The output pins go Low without keeping data when High level is input to the CLR pin described in ***"4.1.1 CLR Pin Function"***.

The Do0 to Do15 pins of the MKY34 have a drive capacity of ±15 mA (max.) and can be connected directly to peripheral components such as transistors, LEDs, and photocouplers.

**Reference**

There is no problem if any unused pins of the Do0 to Do15 pins are left open.

## 3.7 Connection Example of MKY34 Basic Functions

Figure 3.4 shows a connection example of MKY34 basic functions. In the example circuit, all the expanded functions described later are unused. The satellite addresses of the MKY34 can be set by DIP-Switch (DIP-SW).

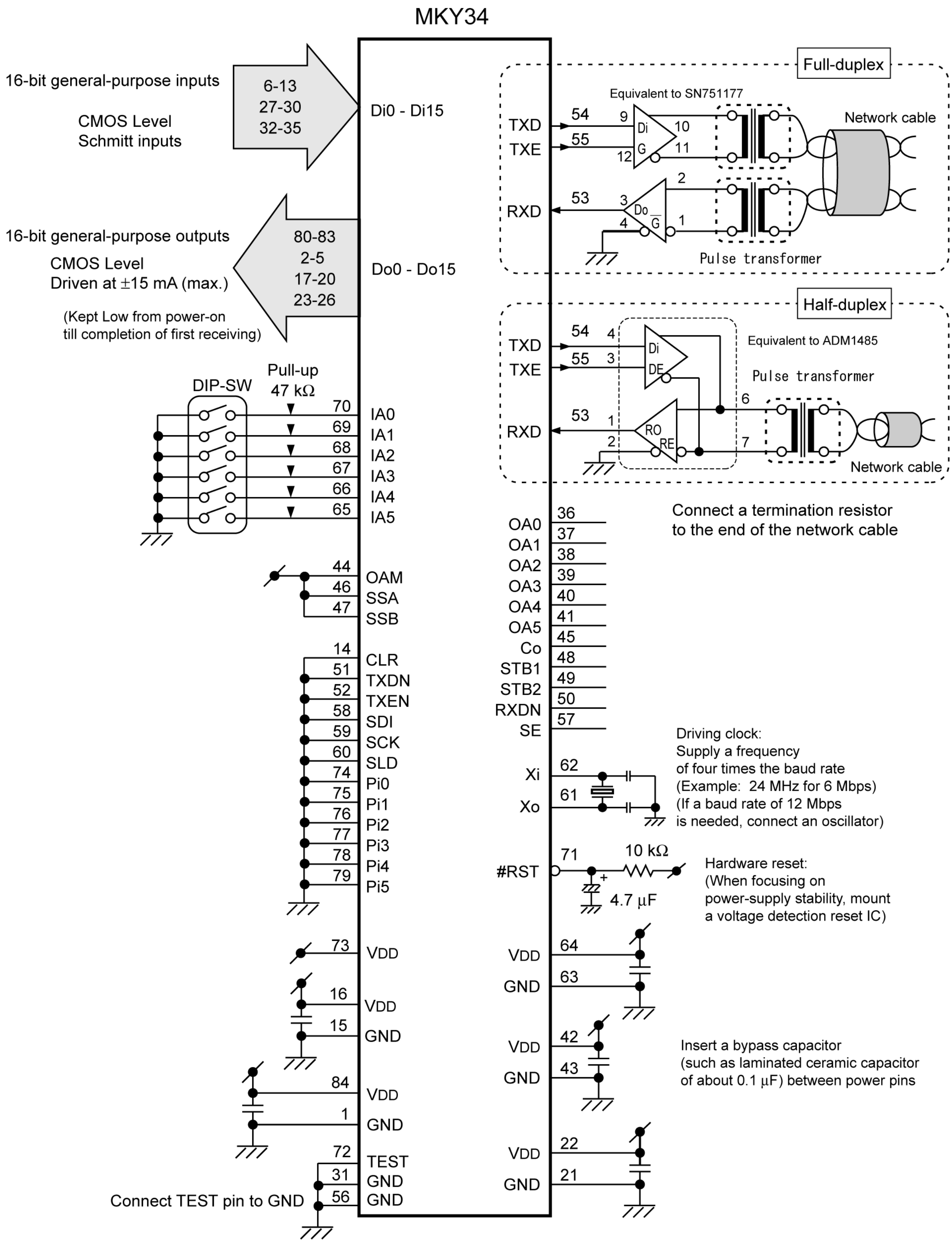



Fig. 3.4 Connection Example of Basic Functions

# Chapter 4 Expanded Functions of MKY34

This chapter describes the pin functions and connections required to operate the expanded functions of the MKY34.

# Chapter 4 Expanded Functions of MKY34

This chapter describes the pin functions and connections required to operate the expanded functions of the MKY34.

Reference

Some expanded functions described in this chapter operate according to the command value in the center IC, which is operated by the user system program. To understand the expanded functions, refer to the description of the control word in ***"User's Manual"*** for the center IC that the MKY34 is connected to.

## 4.1 Setting Strobe Signal and its Application

This section describes how to use the following three functions among the expanded functions described in ***"1.4.2 Expanded Functions"***:

(1) Has CLR pin that sets output pin (Do) Low

(2) Has strobe output pins that indicate timing when to update output pins (Do) and receive input pins (Di)
The user can also design peripheral circuit based on each update timing.

(3) Can set handshake to ensure link with center IC

### 4.1.1 CLR Pin Function

The MKY34 has a CLR (CLeaR) pin (pin 14) that can set forcibly the output pin (Do) Low. When a High level is input to the CLR pin, the states of Do0 to Do15 pins go Low. In normal operation, design so that a Low level is input to the CLR pin.

The state of the MKY34 output pin (Do) is updated each time the MKY34 inputs the command packet (CP) from the center IC transmitted to the address matching the SA set by IA0 to IA5 correctly. However, if scanning is stopped for reasons such as the disconnection of a network cable or center IC faults, the output state of the output pin (Do) is kept continuously. At this time, no strobe signal is output from the STB1 pin, as described in ***"4.1.2 STB1 Pin Function"***. In a user system in which the state of the output pin (Do) is kept inappropriately when scanning is stopped, the MKY34 can use the CLR pin to forcibly clear the state of the output pin (Do) (Low level).

Figure 4.1 shows an example of clearing the state of the output pin (Do) in the watchdog timer circuit using STB1 and CLR signals.

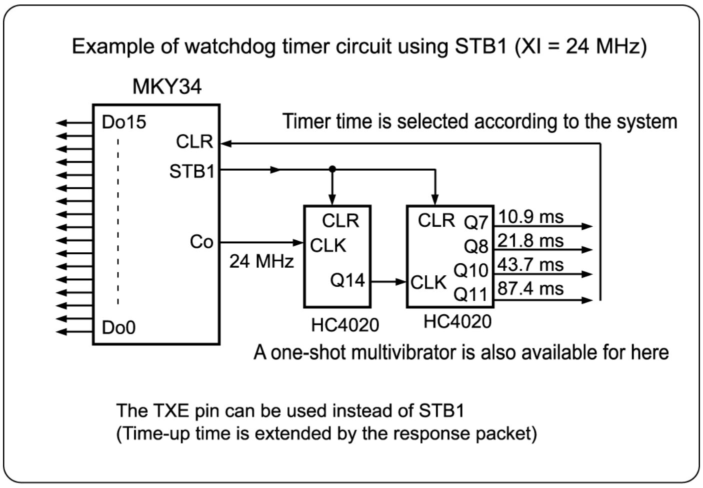



Fig. 4.1 Example of Watchdog Timer Circuit Using STB1

Generally, the time-up time of a watchdog timer needs to be set longer than the allowable time of multiple scan times. However, the time-up time in the example of the watchdog timer circuit shown in Figure 4.1 may be inappropriate in the following cases:

(1) For the user system where HUBs are inserted into network (One scan time increases according to the inserted number of HUBs.)
(2) When user program operating center IC pauses scanning
(3) When user program operating center IC uses single scan and starts single scan according to inappropriate timing for time-up time of watchdog timer
(4) When user program operating center IC stops scanning intentionally

The user should determine whether the time-up time in the example of the watchdog timer circuit shown in Figure 4.1 is appropriate for the user system.

Reference

For details of the scan time, scan pausing, and single scan, refer to the ***"User's Manual"*** for the center IC that the MKY34 is connected to.

Caution

The CLR (CLeaR) pin (pin 14) tends to respond to the High-level input. The Do0 to Do15 pins go Low as soon as a very short High-level pulse including noise is input to the CLR pin.
When designing a user system, prevent High-level signals from entering the CLR pin (by using a capacitor of about 0.1 μF connected to GND near the CLR).

### 4.1.2 STB1 Pin Function

Each time the MKY34 inputs the command packet (CP) matching the SA from the center IC correctly, it outputs data in the CP to the output pin (Do) of the MKY34. The state of the output pin (Do) is updated at the central timing of the pulse-like strobe signal from the STB1 (STroBe-1) pin (pin 48) (Fig. 4.2). The function of this STB1 pin can be used to notify a circuit connected to the output pin (Do) that the output state is updated.

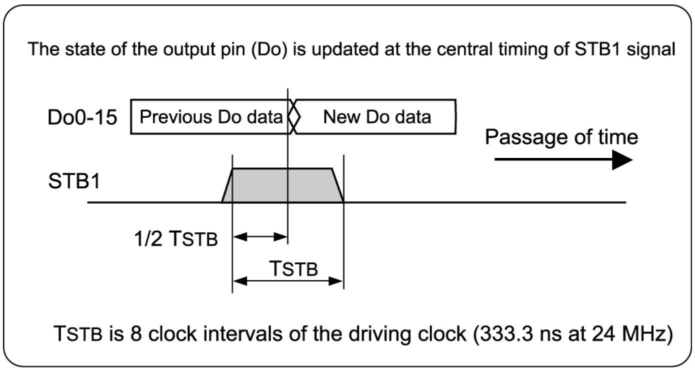



Fig. 4.2 Update Timing of Output Pin (Do)

Reference

The pulse-like strobe signal output from the STB1 pin is unaffected by the command value of the center IC. The strobe signal is also output from the STB1 pin if the state of the output pin (Do) after updating is identical to that before updating.

### 4.1.3 Time to Sample State of Di0 to Di15 Pins (STB2 Pin)

If the command in the CP issued from the center IC is "0" or "8" (basic function specified) when the response packet (RP) is returned in response to the command packet (CP) matching the SA, the MKY34 samples the 16 input pins (Di0 to Di15). The MKY34 outputs a pulse-like strobe signal from the STB2 (STroBe-2) pin (pin 49) to indicate the time to sample the state of the input pin (Di). The state of the input pin (Di) is sampled at the beginning of the strobe signal.

Reference

When the SSB (Strobe Select-B) pin described in ***"4.1.5 Enabling/Disabling Handshake (SSB Pin)"*** is Low, no strobe signal may be output from the STB2 pin when the MKY34 returns the RP.

### 4.1.4 Setting Strobe Signal Timing (SSA Pin)

The following two requests occur in the user system using the HLS:

(1) To update state of output pin (Do) after sampling input state of input pin (Di).

(2) To sample state of input pin (Di) after updating state of output pin (Do).

In the MKY34, the user can select the timing of strobe signals output from the STB1 pin and STB2 pin by setting the SSA (Strobe Select-A) pin (pin 46). This will enable to meet the two requests. The MKY34 performs the operation in (1) above when the SSA pin is set Low, and the operation in (2) above when the SSA pin is set High (Fig. 4.3).

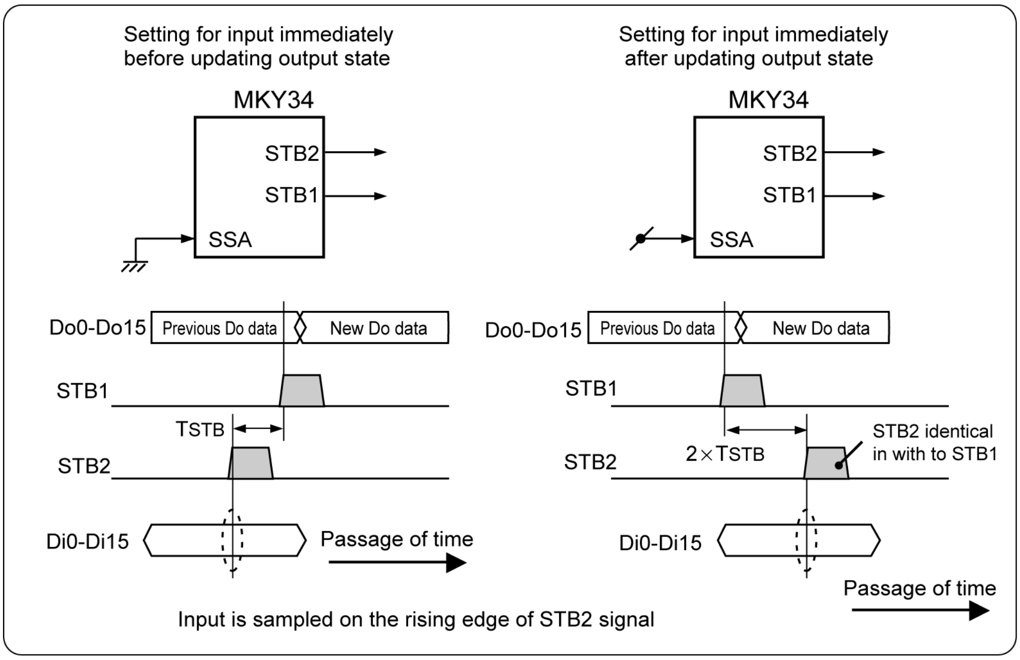



Fig. 4.3 SSA Pin Setting and Update Timing

### 4.1.5 Enabling/Disabling Handshake (SSB Pin)

Handshaking with the center IC can be enabled or disabled by setting the SSB (Strobe Sdect-B) pin (pin 47). When the SSB pin is Low, handshaking with the center IC is enabled.

When the MKY34 inputs the command packet (CP) from the center IC, it recognizes whether the center IC has received correctly the response packet (RP) returned to the center IC at the last scan. In a case where handshaking is enabled, the MKY34 outputs a strobe signal from the STB2 pin to sample the state of the input pin (Di) only when the center IC has input the previously returned RP correctly, and the sampled state of the input pin (Di) is embedded in the RP.

If the center IC has not input the previously returned RP correctly, the MKY34 neither outputs a strobe signal to the STB2 pin nor samples the state of the input pin (Di). In this case, the previously sampled stated of the input pin (Di) is embedded in the RP again. Figure 4.4 shows the timing of generating the STB2 strobe signal in the MKY34 with five satellites and “SA = 2” in half-duplex mode.

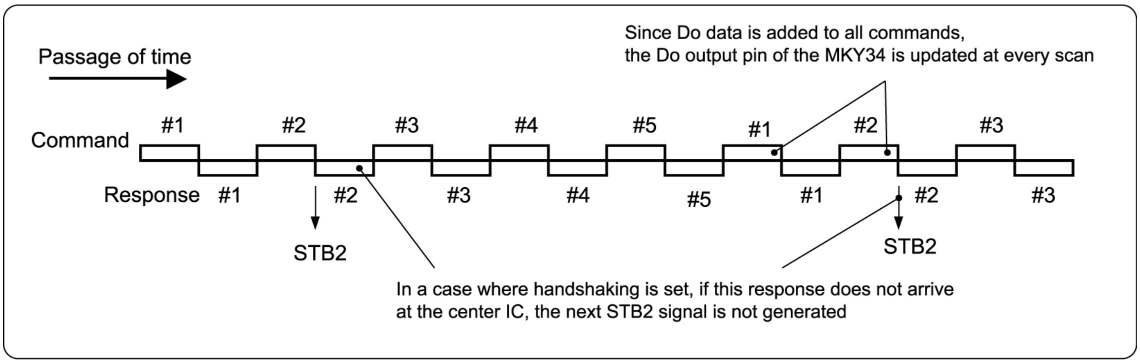



Fig. 4.4 Timing of STB2 Strobe Signal Generation

**Reference** In a user system in which real-timeness is essential when a sensor is connected to the input pin (Di), and so on, disable handshaking.

#### 4.1.5.1 Example of Handshaking Effectiveness

This section describes an example of the effectiveness of handshaking with the center IC.
Some user systems may want to send character string data to the center IC in synchrony with the strobe signal output from the STB2 pin. For example, when transferring character string data consisting of the 5 characters **"ABCDE"** to the input pin (Di) of the MKY34 at each output of the STB2 strobe signal (Fig. 4.5A), a character may be omitted in the character string data obtained by the center IC when handshaking with the center IC is disabled. For example, if there is interference including external noise in the network during sending the letter **"C"** and the RP is discarded at the center IC, the STB2 strobe signal is output at the next scan. Consequently, the center IC receives the character string data **"ABDE"** (**"C"** omitted) (Fig. 4.5B).
In contrast, when handshaking is enabled, the STB2 strobe signal is not output at the next scan even when the RP is discarded at the center IC and character will not be omitted (Fig. 4.5C).

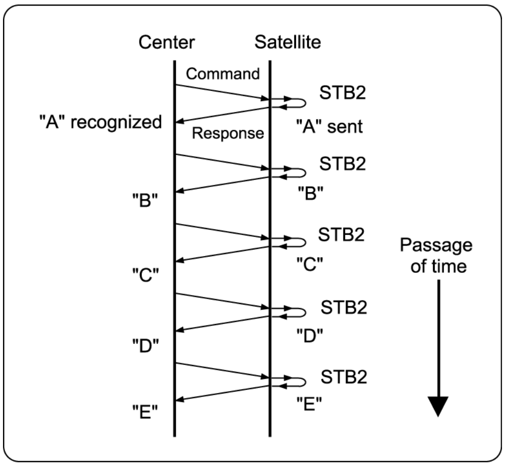



Fig. 4.5A Operation with No Failure

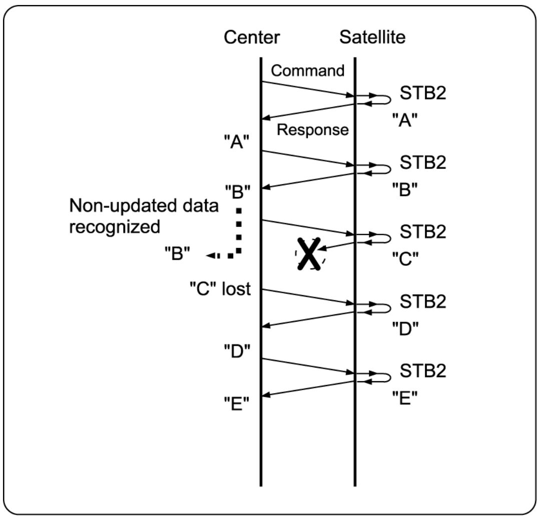



Fig. 4.5B Handshaking Disabled

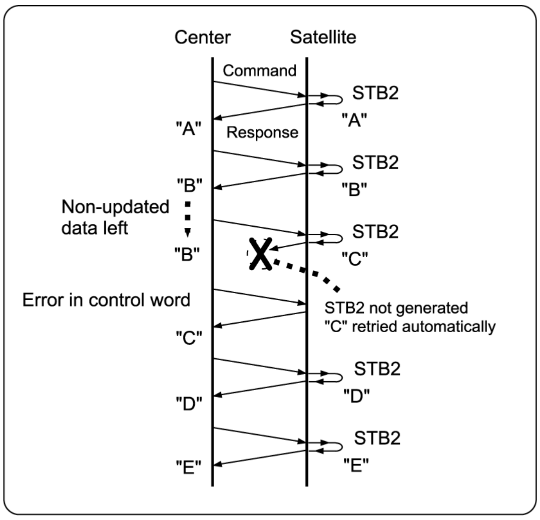



Fig. 4.5C Handshaking Enabled

### 4.1.5.2 Cautions for Sending Character String Data

This section describes the cautions for sending character string data when handshaking is enabled with the SSB pin set Low.
As described previously, enabling handshaking ensures that character string data is sent (without omitting character) to memory in the center IC. In this case, the user system program of the center IC must obtain character string data from memory in synchronization with scan timing. For the example in Figure 4.5C, note the following:

(1) If character string data is simply obtained from memory in synchronization with the scan timing, character string data including duplicated characters like **"ABBCDE"** may be read (because the third character cannot reach at the third scan).
(2) At the third scan, the corresponding satellite IC causes an error (that can be recognized by a nonresponding flag bit in the control word in the center IC).
(3) If the above error occurs, ideally it should be handled by the algorithm that does not read data. However, since scanning is very fast and such handling must be set for each satellite IC, program execution speed may not follow scan speed.

Based on the above cautions, a method for easily creating the program algorithm for the center IC is shown below.
The input pin (Di) consists of 16 pins. If eight pins are used to input a character code (8-bit information), eight pins are left. When a "character counter" is used for these eight input pins (Di), the program algorithm for the center IC can be created easily. Figure 4.6 shows a example of using the high-order one byte (8 bits) of data as a character counter.

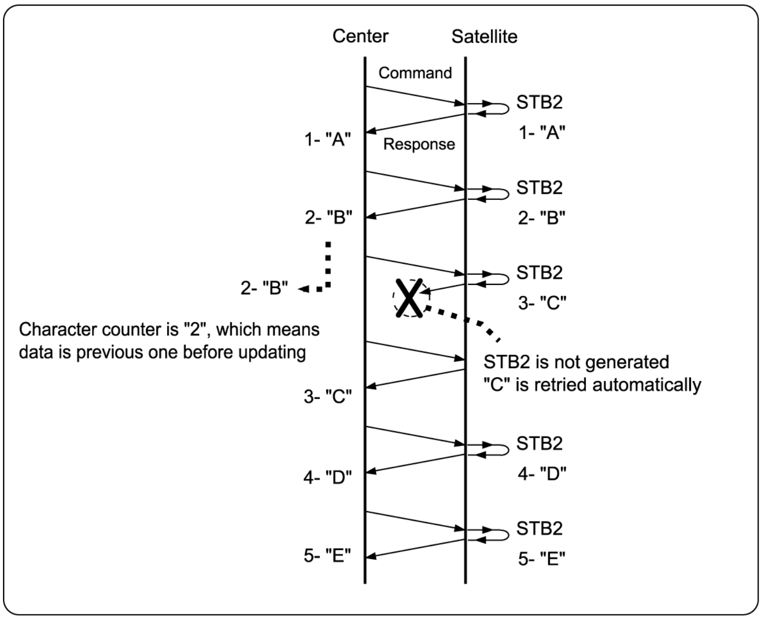



Fig. 4.6 Sending with Character Counter Used

### 4.1.5.3 Caution for Using Handshaking (1)

In the HLS, the handshaking function is intended to send data sampled by the satellite IC to the center IC without loss. This will cause a difference in data arrival at the center IC between when an error occurs in the response packet and when an error occurs in the command packet.
An example of sending character string data is shown. If an error occurs in the response packet (Figs. 4.5C and 4.6), the letter **"C"** does not arrive at link failure and does arrive at the next normal scan. In contrast, if an error occurs in the command packet (Fig. 4.7), the letter **"B"** arrives at the center IC twice at the scan before or after link failure.

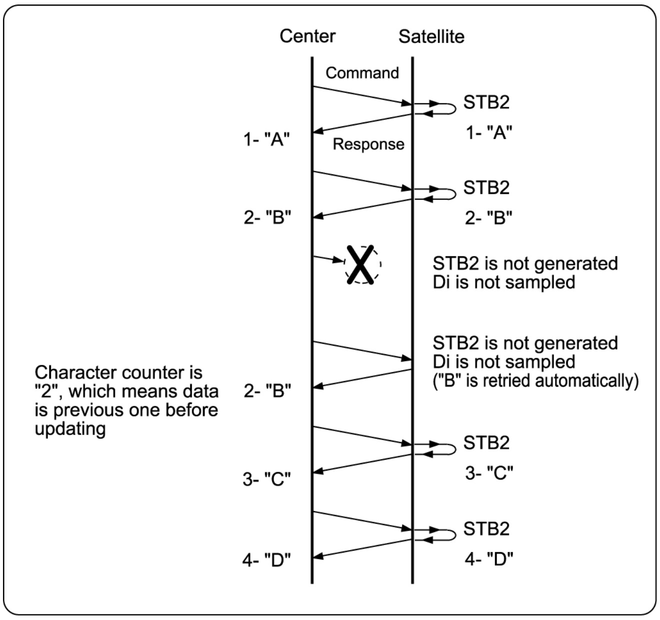



Fig. 4.7 Operation at CP Failure

As shown in this example, in both cases, the data sampled by the satellite IC is sent to the center IC without loss. However, based on the difference in data arrival at the center IC, the user system program must handle data in the center IC (memory). Placing a character counter of at least two or more bits as described in ***"4.1.5.2 Cautions for Sending Character String Data"*** near the MKY34 can help the user system program to deal with to this problem.

### 4.1.5.4 Caution for Using Handshaking (2)

When the SSB pin (pin 47) is set to enable the handshaking, and when the user system executes commands other than “0” or “8” (basic function specified) for the MKY34, no strobe signal is output from the STB2 pin.

Sending character srting data requires some extra time including scanning time during execution of commands other than command “0” or “8”. For example, if the HLS is operated only by command “0” at a baud rate of 6 Mbps, with “FS = 8”, in full-duplex mode, a strobe signal is output from the STB2 pin at an interval of 242 μs.

However, assuming that the HLS is operated with automatic command circulation set by the center IC, the command circulates from “0” to “6” and the output interval of a strobe signal from the STB2 pin seven times longer (1.69 ms) than that at which the HLS is operated only by command “0” (Fig. 4.8).

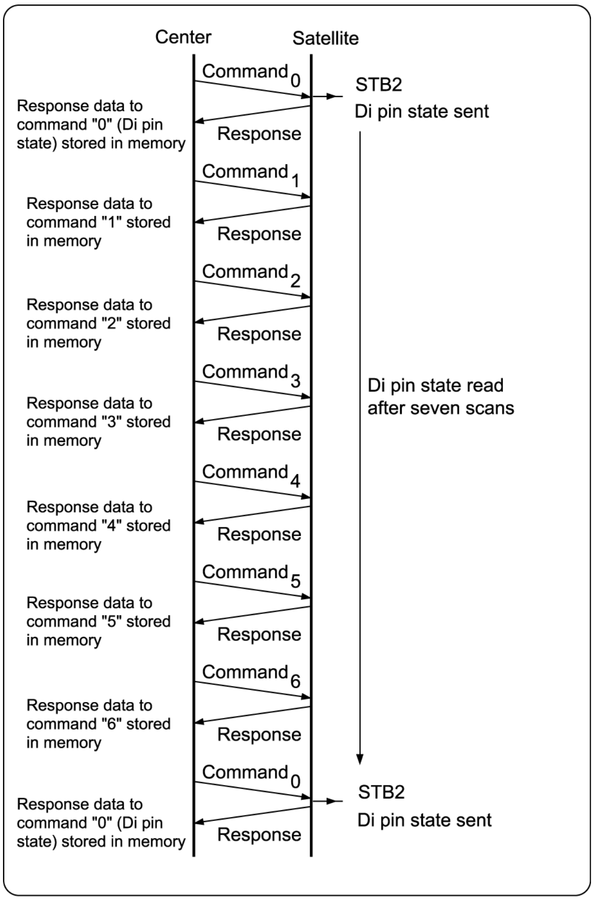



Fig. 4.8 Send of Di Pin State in Command Circulation

## 4.2 Cascade Connection

This section describes ***"(4) Can connect satellite ICs directly by cascade connection"*** in ***"1.4.2 Expanded Functions"***.

### 4.2.1 Cascade Connection Example

Some peripheral components can be reduced when cascade-connecting more than one MKY34.
The MKY34 has dedicated pins that facilitate cascade connection.
Cascade connection of the MKY34 is explained using the example in Figure 4.9.

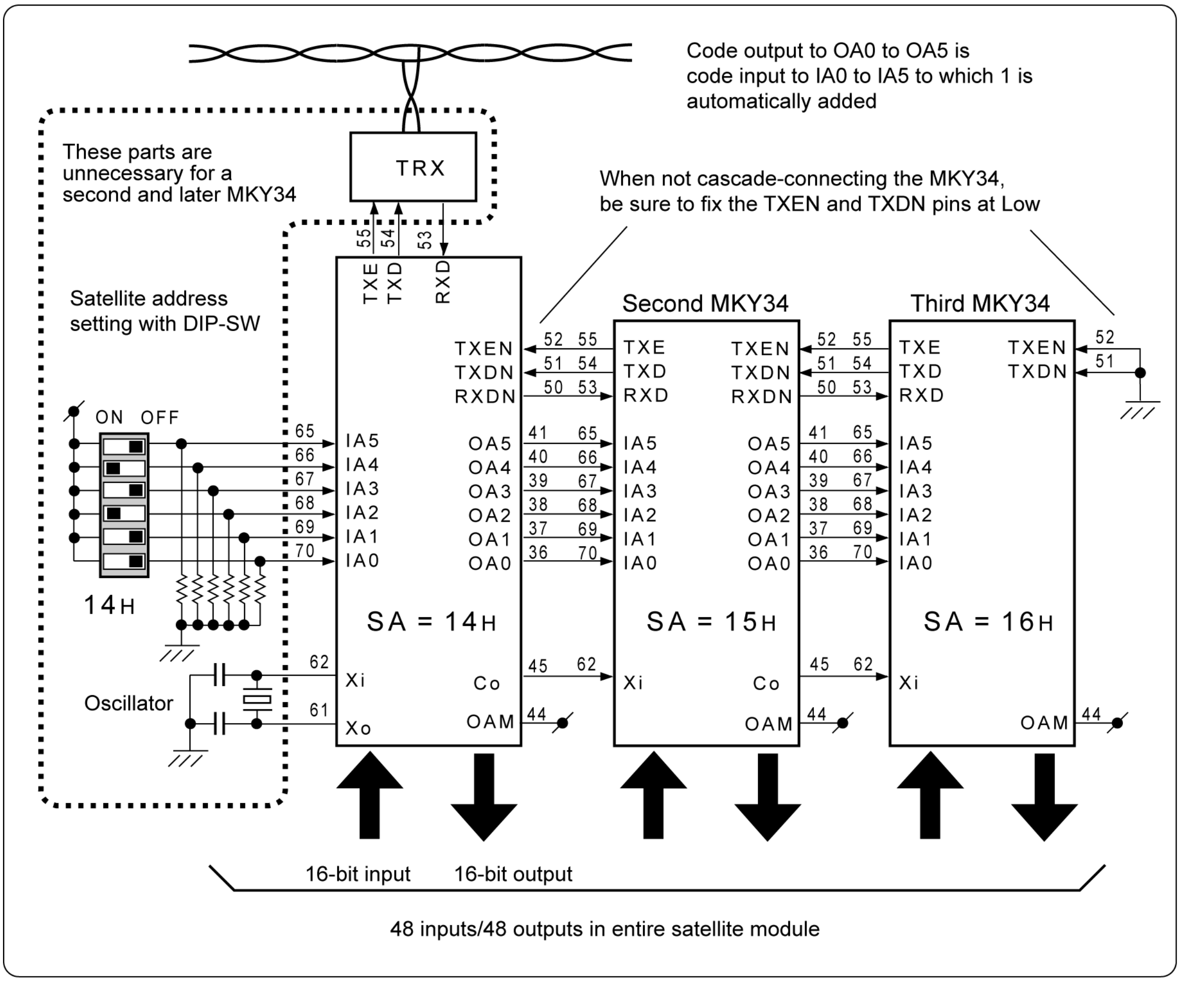



Fig. 4.9 Cascade Connection Example

### 4.2.2 Cascade Connection of SAs

The MKY34 has six pins (OA0 to OA5: Output Addresses 0 to 5) that output the hexadecimal values set at the SA setting pins (IA0 to IA5) with "1" added. By connecting the signals output from IOA0 to OA5 (pins 36 to 41) of the preceding MKY34 directly to IA0 to IA5 of the succeeding MKY34, the succeeding MKY34 can be positioned as the next SA of the preceding MKY34. This cascade connection of satellite addresses eliminates the need for components such as address-setting DIP Switch (DIP-SW) for individual MKY34s, resulting in reduced components.

### 4.2.3 Cascade Connection of Xi Pin

The Co (Clock out) pin (pin 45) of the MKY34 outputs an internally used driving clock. The clock signal output from the Co pin can be connected directly to the Xi pin (pin 62) of the succeeding MKY34. The driving clock output from the Co pin does not stop even when the #RST pin is Low (even when hardware reset is activated). Using this cascade connection of the Xi pin eliminates the need for components including oscillators for individual MKY34s, resulting in reduced components.

### 4.2.4 Cascade Connection of RXD Pin

The serial pattern signal of the CP transmitted by the center IC that is input to the RXD pin is output directly to the RXDN pin (pin 50). The signal output from the RXDN pin can be connected directly to the RXD pin of the succeeding MKY34. Using this cascade connection of the RXD pin simplifies the signal patterns on the circuit board with the MKY34.

### 4.2.5 Cascade Connection of TXE Pin and TXD Pin

When inputting the output signal from the TXD pin of multiple satellite ICs to one TRX driver, as shown in Figure 4.10, the output signals from the TXE pin and TXD pin must be passed through the AND gates and are then synthesized by the OR gates. The active output states of the TXE pin must also be synthesized by the OR gates and then connected to the enable inputs of the TRX driver.

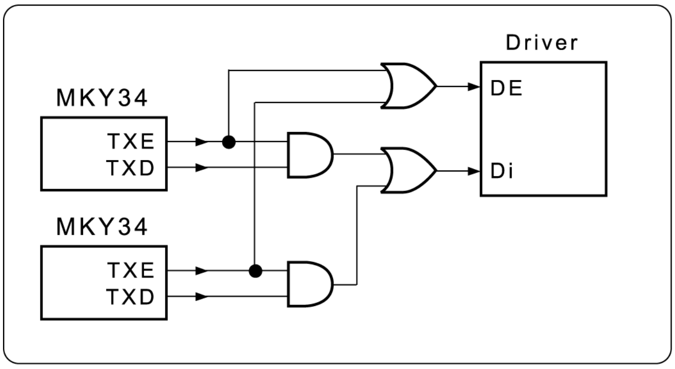



Fig. 4.10 Connection of TXE and TXD Signals of Multiple MKY34s

The MKY34 has a TXEN pin (pin 52) and TXDN pin (pin 51) with circuits equivalent to these AND and OR gates. The output signals from the TXE pin and TXD pin of the succeeding MKY34 can be connected directly to the TXEN pin and TXDN pin of the preceding MKY34 (Fig. 4.9). Using this cascade connection of the TXE pin and TXD pin reduces the number of auxiliary circuit components composed of AND and OR gates (and also eliminates the need for individual satellite ICs to have TRX, resulting in reduced TRXs).

### 4.2.6 Caution for Cascade Connection

(1) Be sure to fix the TXEN pin and TXDN pin of a single MKY34 (without cascade connection) or the last cascade-connected MKY34 at Low. When the TXEN pin goes High during operation, the RP may not be output or may be damaged.

(2) If the frequency of the clock driving the MKY34 is high, the number of nest (Nesting) to which the driving clocks output from the Co pin are cascade-connected to the Xi pin of the subsequent MKY34 should be around three. This is necessary because the duty ratio of clocks passing from the Xi pin to the Co pin in the LSI may change (for example, with a 50-MHz driving clock, the High- or Low-level width is about 10 ns and changes in duty ratio tend to accumulate, causing unstable clock waveforms). If the clock frequency is high and three or more clocks must be connected, the output signal from the first Co pin should be connected to the fourth Xi pin.

(3) Cascade connection of SAs is possible when High is set to the OAM (Out Address Mode) pin (pin 44) of the MKY34. For the conditions to set Low to the OAM pin, refer to ***"4.3.5.1 Digital Filter"***, and ***"4.5.1 Setting Battery-backup Function"***.

(4) In the subsequent MKY34 with "SA = 3FH" (last 63rd), satellite addresses cannot be cascade-connected.

## 4.3 General-purpose 6-channel Counter

This section describes item ***"(5) Has 6-channel 16-bit binary up-counter. The user can use a digital filter to prevent miscounting"*** as described in ***"1.4.2 Expanded Functions"***. The expanded function in this section operates when "1" to "6" or "9" to "E" are specified as the command of the center IC operated by the user system program.

**Reference** To understand this function, refer to the description of the control word in ***"User's Manual"*** for the center IC connecting the MKY34.

### 4.3.1 Function of General-purpose 6-Channel Counter

The 6-channel 16-bit binary up-counter is incremented by "1" each time one Low-to-High change is detected in the signal input to the Pi0 to Pi5 (Pulse input-0 to 5) pins (pins 74 to 79). The counter value ranges from "0" to "65535" (0000H to FFFFH), returning to 0000H from FFFFH. This 6-channel 16-bit binary up-counter is not cleared even if a hardware reset is activated.
Using the backup function described in ***"4.5 Battery-backup Function"***, the value can be kept. Figure 4.11 shows a conceptual diagram for the positioning of the general-purpose 6-channel counter function.

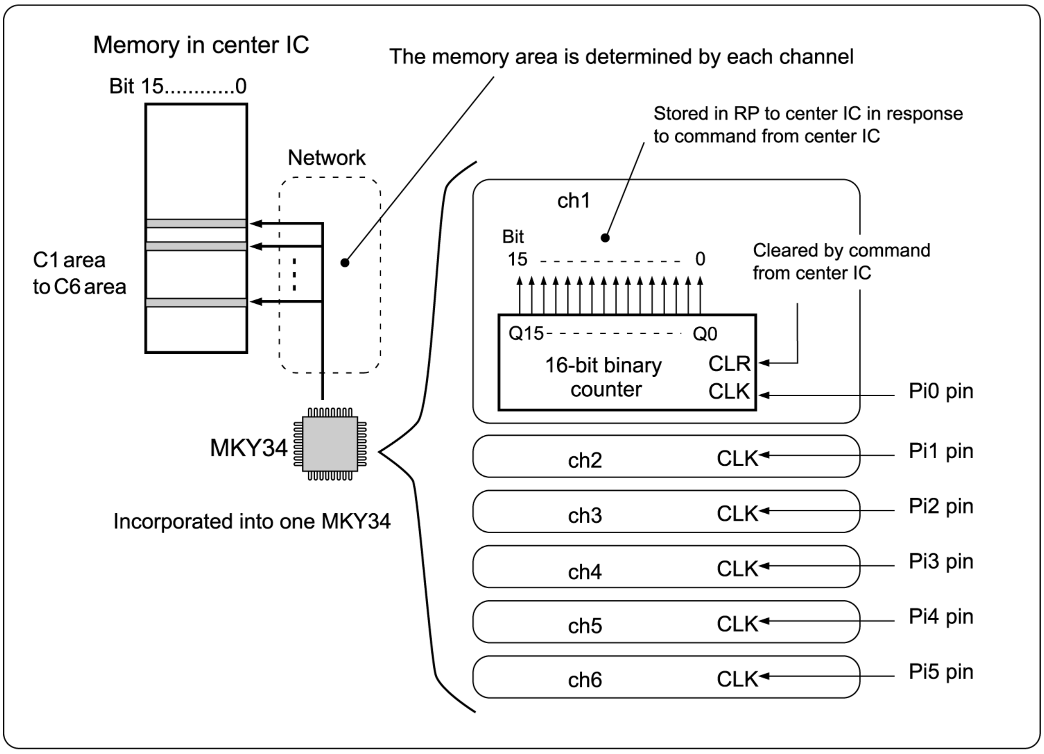



Fig. 4.11 General-purpose 6-channel 16-bit Binary Up-counter

**Caution** When not using the backup function described in ***"4.5 Battery-backup Function"***, the initial counter value is not guaranteed after power-on. In a user system using this function but without using backup function, a command to clear each counter value to 0000H should be issued as initialization by the center IC when the user system is started.

### 4.3.2 Sending and Clearing of General-purpose 6-channel Counter Values

The counter value of each channel is sent to the center IC according to a command issued by the center IC. It can also be cleared to 0000H by a command issued by the center IC.
Table 4-1 lists the functions of the MKY34 for the commands issued by the center IC.

**Table 4-1 Functions of MKY34 Selected by Commands**

| Command | Function of MKY34 | Data stored in response packet | Memory area in center IC |
|---|---|---|---|
| 0 (0H) | Samples Di0 to Di15 pin states | State of Di0 to Di15 pins | Di |
| 1 (1H) | Samples value of counter ch1 | Four-digit hexadecimal value of counter ch1 | C1 |
| 2 (2H) | Samples value of counter ch2 | Four-digit hexadecimal value of counter ch2 | C2 |
| 3 (3H) | Samples value of counter ch3 | Four-digit hexadecimal value of counter ch3 | C3 |
| 4 (4H) | Samples value of counter ch4 | Four-digit hexadecimal value of counter ch4 | C4 |
| 5 (5H) | Samples value of counter ch5 | Four-digit hexadecimal value of counter ch5 | C5 |
| 6 (6H) | Samples value of counter ch6 | Four-digit hexadecimal value of counter ch6 | C6 |
| 7 (7H) | Samples value of SIDR | Value of SIDR (16 bits) | C7 |
| 8 (8H) | Samples Di0 to Di15 pin states | State of Di0 to Di15 pins | Di |
| 9 (9H) | Resets value of counter ch1 to 0000H | 0000H | C1 |
| 10 (AH) | Resets value of counter ch2 to 0000H | 0000H | C2 |
| 11 (BH) | Resets value of counter ch3 to 0000H | 0000H | C3 |
| 12 (CH) | Resets value of counter ch4 to 0000H | 0000H | C4 |
| 13 (DH) | Resets value of counter ch5 to 0000H | 0000H | C5 |
| 14 (EH) | Resets value of counter ch6 to 0000H | 0000H | C6 |
| 15 (FH) | Samples value of SIDR | Value of SIDR (16 bits) | C7 |

### 4.3.3  Input Pins (Pi0 to Pi5 Pins) of Count Signals

The Pi0 to Pi5 pins (pins 74 to 79) of the MKY34 are Schmitt input buffers.  A time-constant circuit to prevent chattering can be connected directly to the Pi0 to Pi5 pins.  Fix the unused pins of the Pi0 to Pi5 pins at High or Low.  A pull-up or pull-down resistor should be connected to pins reserved for future use.
Figure 4.12 shows an equivalent circuit in the MKY34 where signals input from the Pi0 to Pi5 pins reach the count-up input of the counter.  Passage of signals input from the Pi0 to Pi5 pins through a digital filter is determined according to the setting of the OAM (Out Address Mode) pin (pin 44).

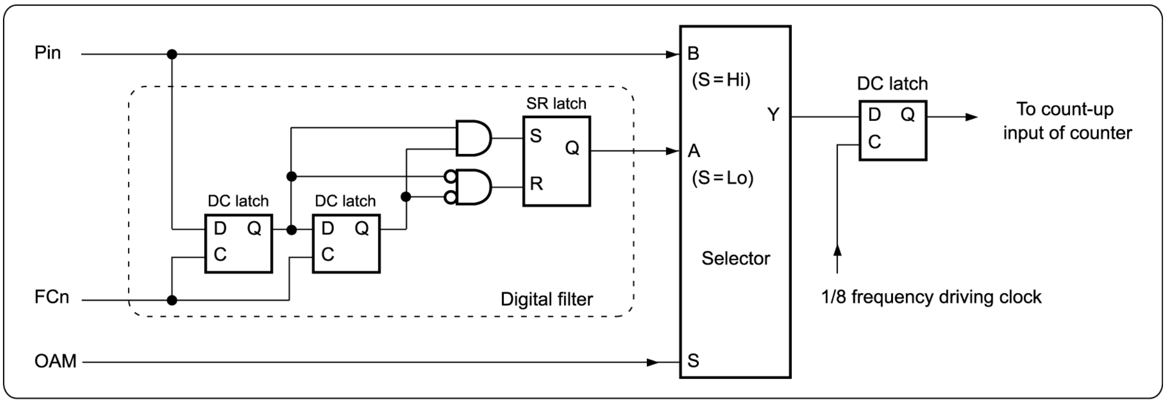



Fig. 4.12   Equivalent Circuit in MKY34 where Signals Reach Count-up Input

### 4.3.4  Counting with OAM Pin Set High

When the OAM pin is set High (signal of selector B shown in Figure 4.12 selected), the signal input to the Pi pin is connected to the input of the DC latch via the selector.  The DC latch samples the input on the rising edge of the "1/8 (divide-by-8)" frequency driving clock.  When the output of the DC latch changes from Low to High, the value of the 16-bit binary up-counter is incremented by "1" (Fig.4.13).

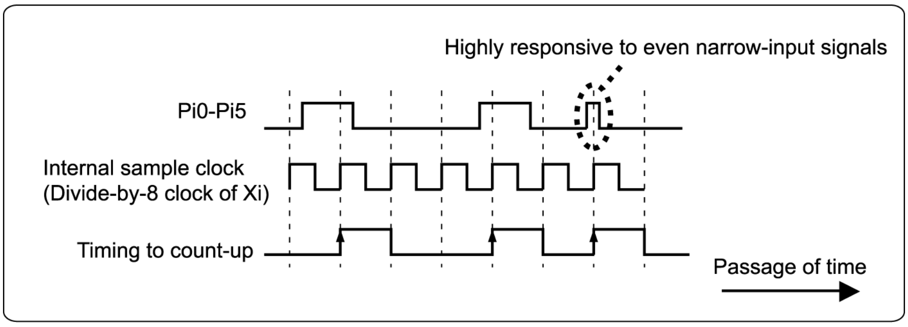



Fig. 4.13   Counting with OAM Pin Set High

Consequently, the input signals to the Pi pin that can be counted should have a longer High level and Low level than $8T_{XI}$ time (Xi = 48 MHz:  about 167 ns).

- **Example 1:** When the baud rate is 12 Mbps (Xi = 48 MHz), the upper limit is 3 MHz (duty ratio 50%:  pulse width about 167 ns).
- **Example 2:** When the baud rate is 6 Mbps (Xi = 24 MHz), the upper limit is 1.5 MHz (duty ratio 50%:  pulse width about 334 ns).

### 4.3.5 Counting with OAM Pin Set Low

When the OAM pin is set Low (signal of selector A in Figure 4.12 selected), a digital filter in the MKY34 is inserted (Fig. 4.12).

#### 4.3.5.1 Digital Filter

Figure 4.14 shows the concept of the digital filter operation. The digital filter operates with a clock (called a "filter clock" and it differs from a driving clock) of any frequency supplied to the FC1 to FC3 (Filter Clock-1 to -3) pins (pins 36 to 38). It consists of two-stages of shift registers. The two-stages of shift registers sample the signal input to the Pi pin according to the rising edge of the filter clock.

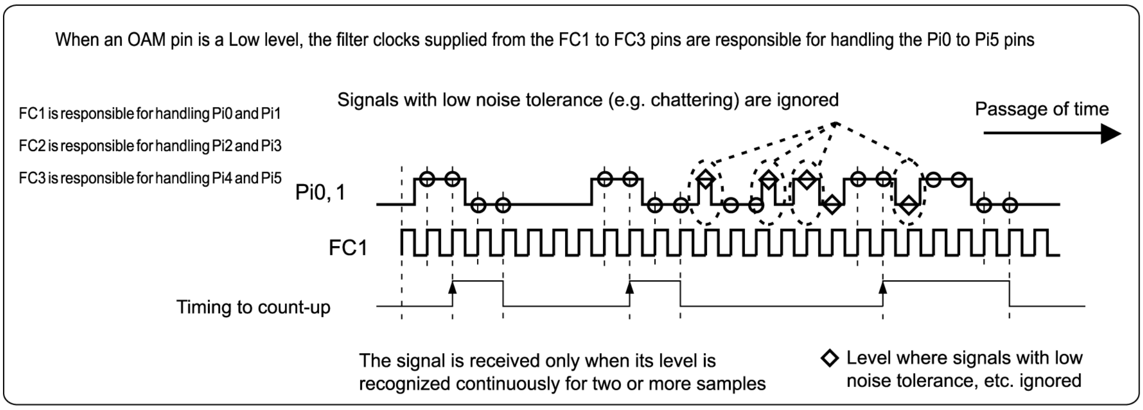



Fig. 4.14 Digital Filter Circuit Operation

By the digital-filter function, the signal input to the Pi pin is recognized to be correct High level only when it is kept High continuously for two or more clocks of the filter clock. The same is true for recognition of a Low level. Signals passed through the digital filter are shaped into signals with high noise tolerance because low noise level change are removed. The digital filter supplied with a filter clock of the correct frequency can be used for a user system in which the user can arbitrarily select to prevent count errors caused by noise and small level changes.

When the OAM pin is set Low (signal of selector A in Figure 4.12 selected), the output of the digital filter is connected to the input of the DC latch via the selector. The DC latch samples the input on the rising edge of the "1/8 (divide-by-8)" frequency driving clock. When the output of the DC latch changes from Low to High, the value of the 16-bit binary up-counter is incremented by "1".

Consequently, input signals to the Pi pin that can be counted should have a longer High-level and Low-level width than two periods of the filter clock and 8TXI time (Xi = 48 MHz: about 167 ns).

**Caution**

When Low is set to the OAM pin, the backup function described in ***"4.5 Battery-backup Function"*** is also selected. Set the STOP pin (pin 39) Low. While the STOP pin is High, the MKY34 enters the backup mode and all operations stop.
When using the cascade connection of SAs described in ***"4.2.2 Cascade Connection of SAs"***, High is set to the OAM pin of the MKY34 and no digital filter can be inserted.

### 4.3.5.2 Use of Digital Filters

The digital filter for the Pi0 and Pi1 pins (pins 74 and 75) functions by supplying a filter clock to the FC1 pin (pin 36). The digital filter for the Pi2 and Pi3 pins (pins 76 and 77) functions by supplying a filter clock to the FC2 pin (pin 37). The digital filter for the Pi4 and Pi5 pins (pins 78 and 79) functions by supplying a filter clock to the FC3 pin (pin 38). The digital filters can be divided into three groups for insertion according to the target counter (Fig. 4.15).

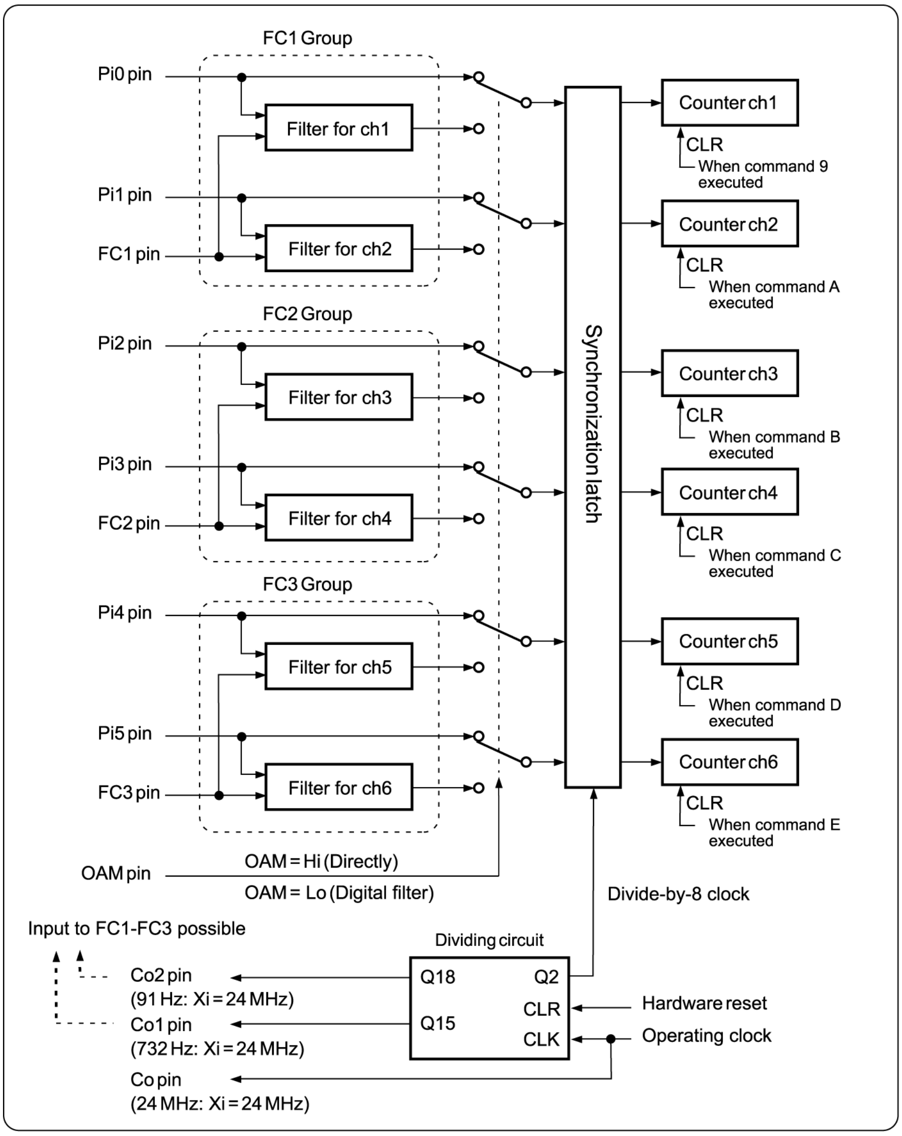



Fig. 4.15 Block Diagram of Counter Function

#### 4.3.5.3 Signal Source of Filter Clock

In the user system, either an oscillator of the correct frequency or an auxiliary clock output signal from the MKY34 can be used as the signal source for the filter clock. The "1/32768 (divide-by-$2^{15}$)" frequency of the driving clock input to the Xi pin is output from the Co1 pin (pin 40) of the MKY34, and the "1/262144 (divide-by-$2^{18}$)" frequency is output from the Co2 pin (pin 41) (Fig. 4.15). The clock signal output from the Co1 or Co2 pin can be used directly as the signal source for the filter clock. This clock signal can also be used for purposes other than the signal source of the filter clock.

**Caution** The clocks output from the Co1 and Co2 pins stop when a hardware reset is activated.

#### 4.3.5.4 Examples of Selection of Filter Clock Frequencies

Examples of selection of filter clock frequencies are shown below.

- **Example 1: Counting push-button switches**
  Counting switches that may cause chattering of less than 20 ms requires a filter clock of more than 10 ms (less than 100 Hz). If the MKY34 has a baud rate of 6 Mbps, a 91-Hz clock signal is output from the Co2 pin and can be used as the signal source for the filter clock.

- **Example 2: Counting pulse signal of about 10 ms generated by photo-interrupter unaffected by external noise (about 2-ms pulse)**
  This requires a filter clock of more than 1 ms (less than 1 kHz). If the MKY34 has a baud rate of 6 Mbps, a 732-Hz clock signal is output from the Co2 pin and can be used as the signal source for the filter clock.

- **Example 3: Counting number of ON times of mechanical contact**
  If chattering of less than 150 ms may occur in a mechanical contact, a filter clock of about 75 ms (less than 13.3 Hz) is required. If the MKY34 has a baud rate of 6 Mbps, an about 11.4 Hz (about 88 ms) clock can be generated by frequency-dividing a 91-Hz clock signal output from the Co2 pin into "1/8" with another logic component. This clock can be used as the signal source for the filter clock to remove chattering of less than about 176 ms.

## 4.4 Serial ID Send Function

This section describes item ***"(6) Has 16-bit Serial IDentification Register (SIDR)"*** described in section ***"1.4.2 Expanded Functions"***. The expanded function in this section operates when "7" and "F" are specified as the command of the center IC operated by the user system program.

Reference

To understand this function, refer to the description of the control word in ***"User's Manual"*** for the center IC connecting the MKY34.

### 4.4.1 Applications of Serial ID Send Function

The input pin (Di) and output pin (Do) of the MKY34 are usually I/O ports that are to be controlled by the user system program operating the center IC. In contrast, the serial ID send function allows sending IDentification codes (such as ID data) to the center IC. Traditionally, the user system that identifies an object by ID codes had to have a network for remote control and a network line to send data including ID codes, separately. In addition, the center equipment of the user system had to have the capability to operate these dissimilar networks individually. The MKY34 provides expanded functions that enable integrated operations under these conditions (Fig. 4.16).

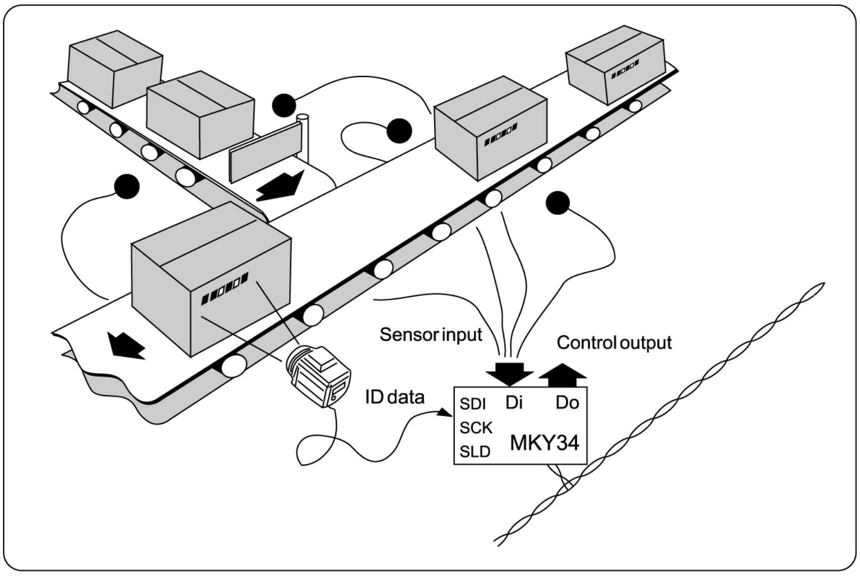



Fig. 4.16 Example of Use of Serial ID Send Function

### 4.4.2 Overview of Serial ID Send Function

IDentification codes are input serially to the 16-bit Serial IDentification Register (SIDR) in the MKY34 from the SDI pin (pin 58), SCK pin (pin 59), and SLD pin (pin 60). The succeeding input is not accepted until the ID codes input to the SIDR information are correctly to the center IC after the MKY34 receives command packet (CP) of command "7" or command "F". The SE pin (pin 57) of the MKY34 outputs the status indicating that IDentification codes are input to the SIDR (SE pin = Low) or that the SIDR is ready to accept input (SE pin = High).

### 4.4.3 Procedure for Use of Serial ID Send Function

This section describes the procedure for use of the serial ID send function. See Figure 4.17.

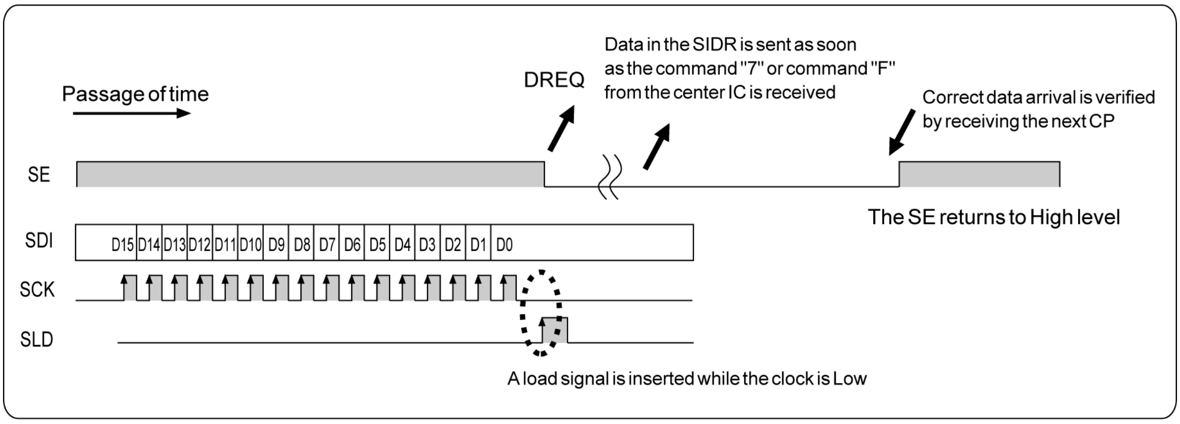



Fig. 4.17 Procedure for Use of Serial ID Send Function

(1) IDentification codes can be input to the SIDR in the MKY34 only when the SE pin (pin 57) is High. When the SE pin is Low, signal input to SDI, SCK, and SLD pins is ignored.

(2) The SDI and SCK pins are input pins for the SIDR in the MKY34. The state of the SDI pin is read to the SIDR consisting of 16-bit shift registers in synchronization with the rising edge of the clock supplied to the SCK pin. If the rising edge of the clock is less than 16 times, some previous information of the SIDR remains shifted in the high-order bit. If the rising edge of the clock is more than 16 times, information overflow to the higher bit is discarded.

(3) When the rising edge signal is input to the SLD pin, the MKY34 recognizes the completion of setting to the SIDR. The SE pin of the MKY34 keeps Low to notify that the serial ID send function has started. This causes a DREQ (Data REQuest) signal to be generated as a serial ID send request to the center IC and is also notified to the user system program operating the center IC.

(4) Design a user system program operating the center IC so that the center IC issues command “7” or command “F” to permit sending of SIDR information when a serial ID send request from the MKY34 is detected.

(5) In response to the CP for command “7” or command “F” issued from the center IC, the MKY34 returns the RP containing SIDR information to the center IC.

(6) Design a user system program operating the center IC so that the center IC reads SIDR information obtained from the C7 area after returning to command “0”.

(7) After completing correct sending of SIDR information to the center IC, the MKY34 changes the SE pin from Low to High and completes one serial ID send function.

**Reference**

Sending and receiving between the center IC and MKY34 corresponding to command “7” or command “F” is protected by handshaking. Therefore, even if the CP or RP is damaged by some failure (including external noise), the serial ID send function is completed correctly by the center IC retry.

### 4.4.4 Caution for Using Serial ID Send Function

This section describes the caution for using the serial ID send function.

(1) The SIDR is backed-up by a battery. Consequently, once started, the serial ID send function does not stop even if an MKY34 hardware reset is activated. (The function can be terminated only by command “7” or command “F” issued from the center IC.)

(2) When inputting a rising-edge signal to the SLD pin, set the SCK pin Low. If a rising-edge signal is input to the SLD pin when the SCK pin is High, one more bit of the state of the SDI pin is read to the SIDR, consisting of shift registers.

(3) The SDI, SCK, and SLD pins have a Schmitt type input buffer. The SCK and SLD pins are triggered on the edge of the signal. A time-constant circuit can be connect near these pins to prevent input of illegal external edge signals to them.

(4) When not using the serial ID send function, keep the SDI and SCK pins High or Low, and the SLD pin Low.

(5) The frequency of the clock supplied to the SCK pin must be lower than the frequency supplied to the Xi pin.

(6) In an MKY34 that is not protected by a backup battery, the serial ID send function may be started at power-on even if the function is not used. This event is the same state as where a rising-edge signal is input to the SLD pin within the MKY34 due to abnormal event (including drift in power supply to power pins) after the MKY34 is turned on. In a user system that must deal with an unintended start of the serial ID send function when the MKY34 is powered on, use the user system program operating the center IC to issue dummy command “7”.

    In a backup-battery-protected MKY34, an unintended start of the serial ID send function never occurs when the MKY34 is powered on if countermeasures to prevent input of an invalid rising-edge signal to the SLD pin are taken in the circuit connected to the MKY34.

## 4.5 Battery-backup Function

This section describes the item ***"(7) Can backup 6-channel 16-bit binary counter and SIDR values by using battery"*** described in section ***"1.4.2 Expanded Functions"***.

### 4.5.1 Setting Battery-backup Function

When a High-level signal is input to the STOP pin (pin 39) while the OAM pin (pin 44) is Low, the values of the 6-channel 16-bit binary up-counter and the SIDR can be kept in the MKY34 by the backup-battery power. Figure 4.18 shows a conceptual diagram of the peripheral circuit for battery-backup of the MKY34.

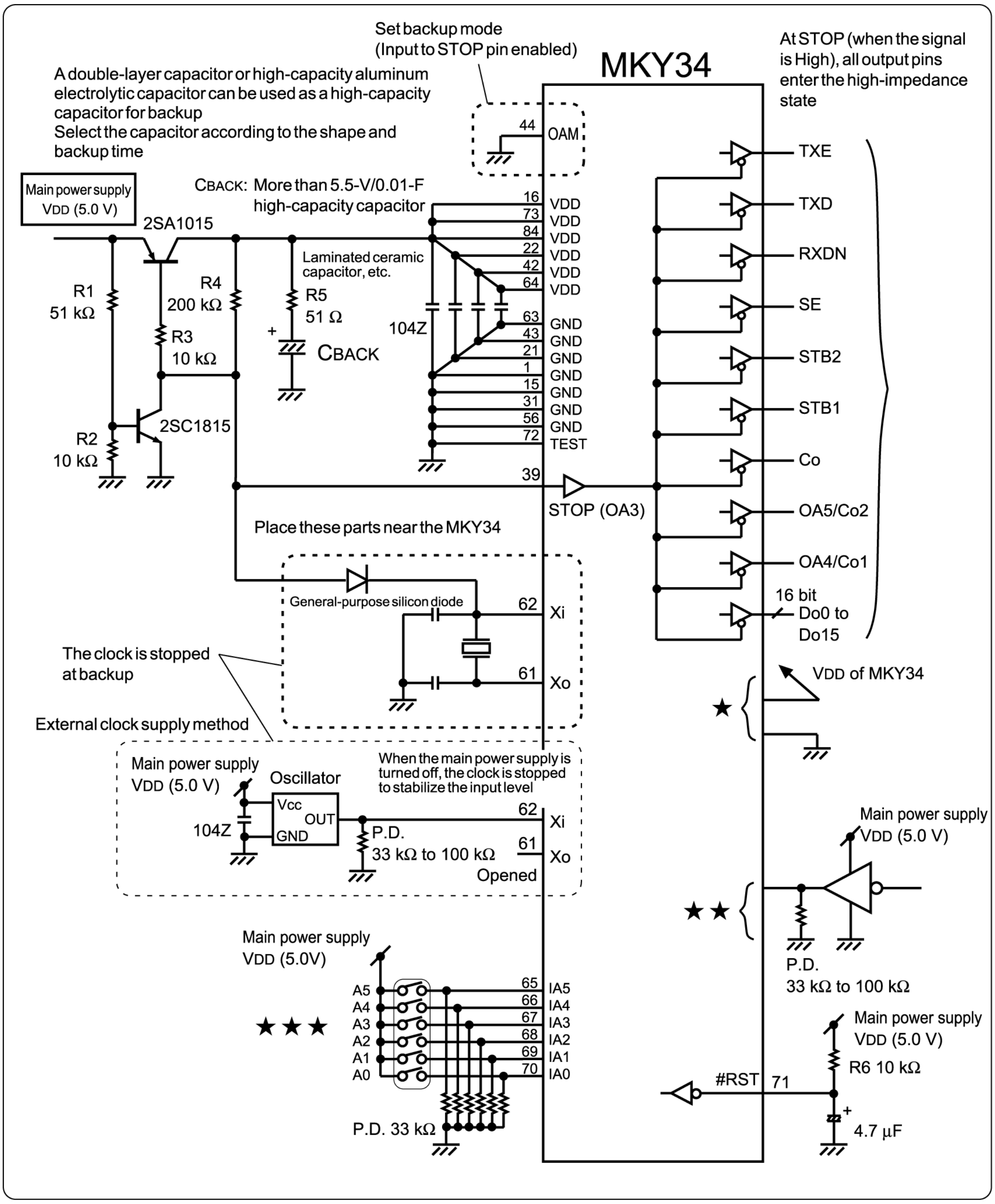



Fig. 4.18 Conceptual Diagram of Peripheral Circuits for MKY34 Battery-backup

## 4.5.2 Operation and Connection for Battery-backup

When the MKY34 enters the backup mode, all output pins enter the high-impedance state and all functions enter sleep mode. For battery-backup, follow the following pin connections:

(1) Stop clock input in the Xi pin (pin 62) to reduce consumption current.

(2) Fix the unused input pin (indicated by ★ in Figure 4.18) at non-active level (High or Low). Pins that keep High keep even when the main power supply is turned OFF, connect it to the VDD pin of the MKY34 where battery voltage is applied, instead of to the VDD pin of the main power supply.

(3) Insert a pull-down resistor so that the input pin (indicated by ★★ in Figure 4.18) where a signal from a component driven by the main power supply is connected does not enter the high-impedance state even if the main power supply is turned OFF.

(4) Design so that the input pins (indicated by ★★★ in Figure 4.18) connected to mechanical switches such as the IA0 to IA5 pins are kept Low by pull-down resistors when the switches are open.

## 4.5.3 Guaranteed Backup Voltage and Backup Time Measurement

The guaranteed backup voltage of the MKY34 is 2.50 V. If the voltage of the VDD pin of the MKY34 falls below 2.50 V, the values of the 6-channel 16-bit binary up-counter or the SIDR in the MKY34 are not guaranteed.

Figure 4.19 shows the circuit with the MKY34 for measuring battery-backup time (the battery-backup consumption current is 9 µA) and Table 4-2 shows the results of measuring the battery-backup time. Assuming a relatively short hours of battery-backup in the event of a short power interruption, the circuit in Figure 4.19 uses a high-capacity capacitor, so the battery-backup time is several hours. To keep a long hours of backup, use large-capacity batteries such as lithium-ion or nickel-cadmium batteries.

**Table 4-2 Measurement Results of Battery-backup Time**

(Unit: V)

| | 1 h | | 2 h | | 3 h | | 5 h | | 7 h | | 9 h | | 12 h | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CBACK | Point A | Point B | Point A | Point B | Point A | Point B | Point A | Point B | Point A | Point B | Point A | Point B | Point A | Point B |
| NEC FYLOH103Z 5.5 V 0.01F | 3.28 | 2.90 | 2.78 | 2.52 | 2.52 | 2.32 | ---- | ---- | ---- | ---- | ---- | ---- | ---- | ---- |
| NEC FYLOH223Z 5.5 V 0.022F | 3.68 | 3.20 | 3.30 | 2.90 | 3.16 | 2.80 | 2.81 | 2.54 | 2.61 | 2.38 | ---- | ---- | ---- | ---- |
| NEC FYLOH473Z 5.5 V 0.047F | 3.94 | 3.43 | 3.58 | 3.11 | 3.38 | 2.96 | 2.99 | 2.67 | 2.80 | 2.54 | 2.61 | 2.40 | 2.42 | 2.24 |

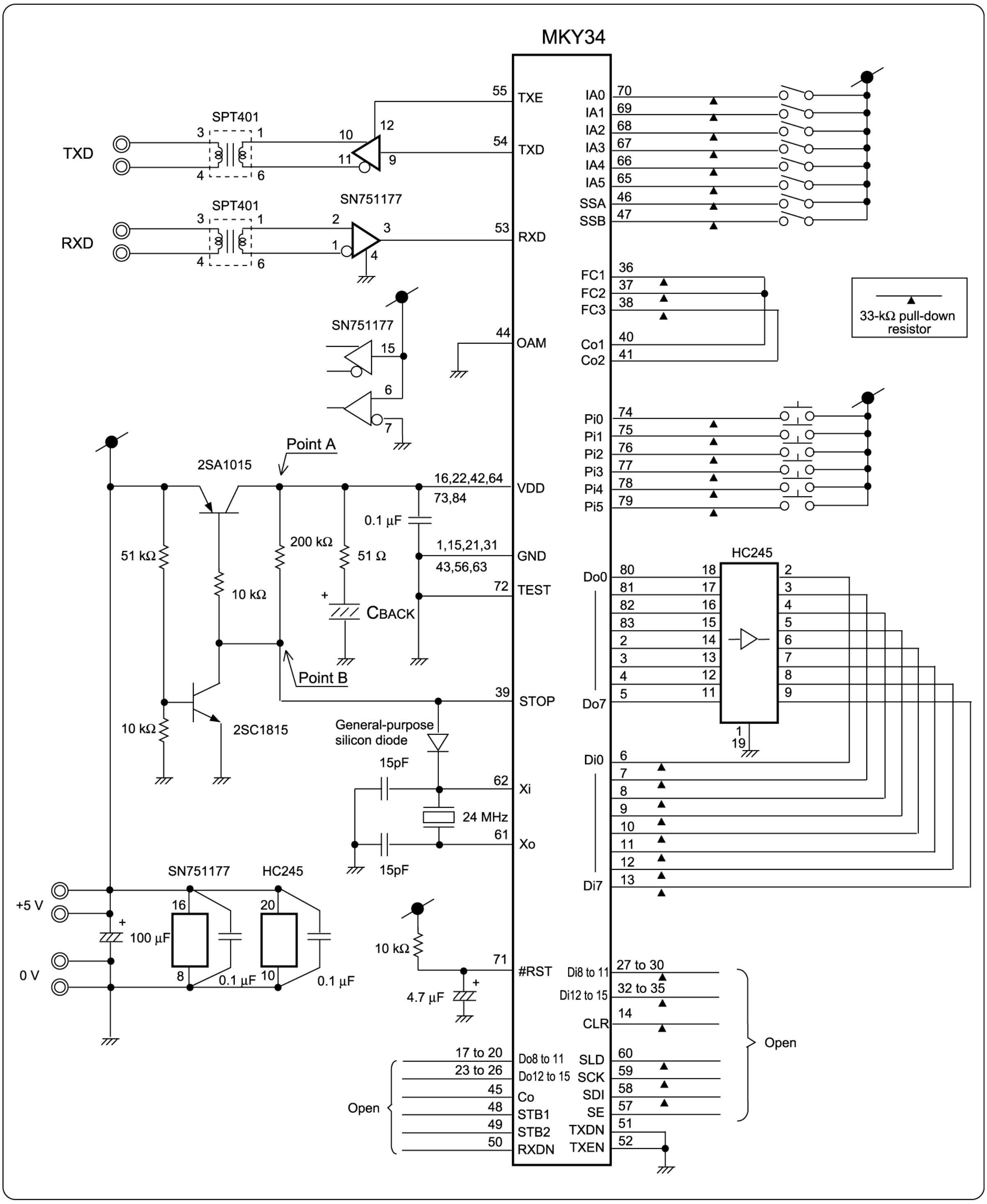



Fig. 4.19 Circuit for Measuring Battery-backup Time

# Chapter 5 Ratings

This chapter describes the ratings of the MKY34.

# Chapter 5 Ratings

This chapter describes the ratings of the MKY34.

## 5.1 Electrical Ratings

Table 5-1 lists the absolute maximum ratings of the MKY34.

**Table 5-1 Absolute Maximum Ratings**

(Vss = 0 V)

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Power supply voltage | $V_{DD}$ | -0.3 to +7.0 | V |
| Input voltage | Vi | $V_{SS}$-0.3 to $V_{DD}$+0.3 | V |
| Output voltage | Vo | $V_{SS}$-0.3 to $V_{DD}$+0.3 | V |
| Peak output current (Not Type A) | Iop | Peak ±20 | mA |
| Peak output current (Type A) | Iop | Peak ±40 | mA |
| Allowable power dissipation | PT | 570 | mW |
| Operating temperature | Topr | -40 to +85 | °C |
| Storage temperature | Tstg | -55 to +150 | °C |

Table 5-2 lists the electrical ratings of the MKY34.

**Table 5-2 Electrical Ratings**

($T_A$ = 25 °C Vss = 0 V)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating power supply voltage | $V_{DD}$ | --- | 4.5 | 5.0 | 5.5 | V |
| Mean operating current | $V_{DD}$A | Vi = $V_{DD}$ or Vss<br>Xi = 50 MHz output open | --- | 50 | 100 | mA |
| | | Vi = $V_{DD}$ or Vss<br>Xi = 24 MHz output open | --- | 25 | 50 | mA |
| External input frequency | Fclk | Input to Xi pin | --- | --- | 50 | MHz |
| Oscillation operating frequency | Fosc | Xi, Xo oscillator connecting | 4 | 24 | 30 | MHz |
| Oscillation feedback resistance | Rfb | $V_I$ = $V_{DD}$ or $V_{SS}$<br>$V_{DD}$ = 5.0 V | 260 | 650 | 1600 | kΩ |
| Input pin capacitance | Ci | $V_{DD}$ = Vi = 0 V<br>f = 1 MHz $T_A$ = 25°C | --- | 7 | 15 | pF |
| Output pin capacitance | Co | | --- | 7 | 15 | pF |
| I/O pin capacitance | Ci/o | | --- | 7 | 15 | pF |
| Rise/fall time of input signal | $T_{IRF}$ | --- | --- | --- | 100 | ns |
| Rise/fall time of input signal | $T_{IRF}$ | Schmidt trigger input | --- | --- | 50 | ms |

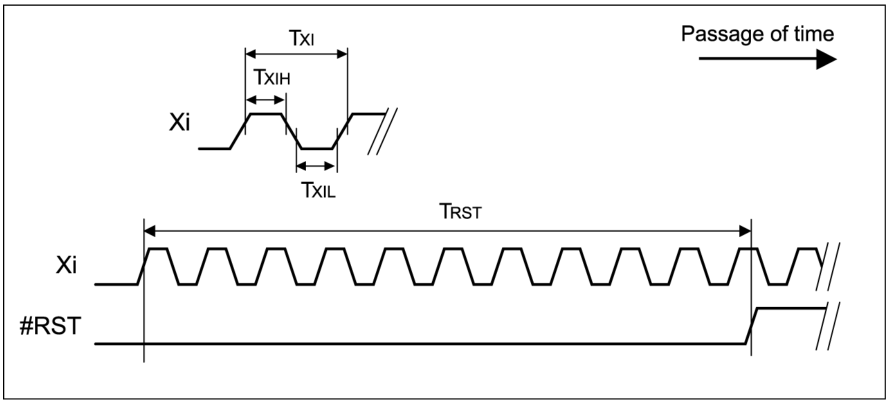
## 5.2 AC Characteristics

Table 5-3 lists the measurement conditions for AC characteristics of the MKY34.

**Table 5-3 AC Characteristics Measurement Conditions**

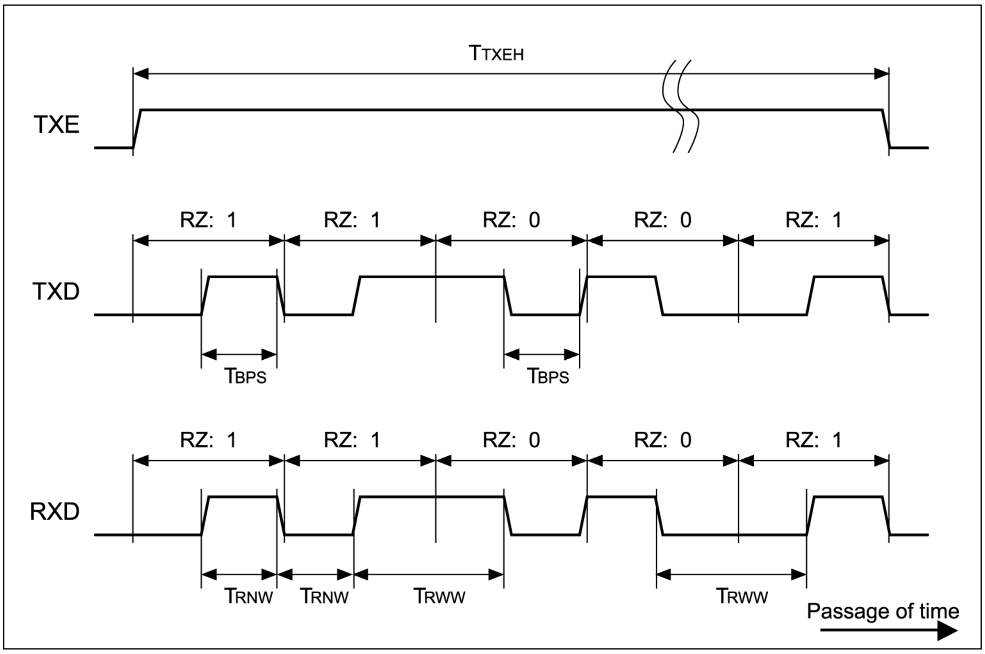
| Symbol | Name | Value | Unit |
|---|---|---|---|
| COL | Output load capacitance | 85 | pF |
| VDD | Power supply voltage | 5.0 | V |
| TA | Temperature | 25 | °C |

### 5.2.1 Clock and Reset Timing (#RST, Xi)




| Symbol | Name | Min. | Max. | Unit |
|---|---|---|---|---|
| TXI | Clock period width | 20 | --- | ns |
| TXIH | Clock High level width | 5 | --- | ns |
| TXIL | Clock Low level width | 5 | --- | ns |
| TRST | Reset enable Low level width | 10 × TXI | --- | ns |

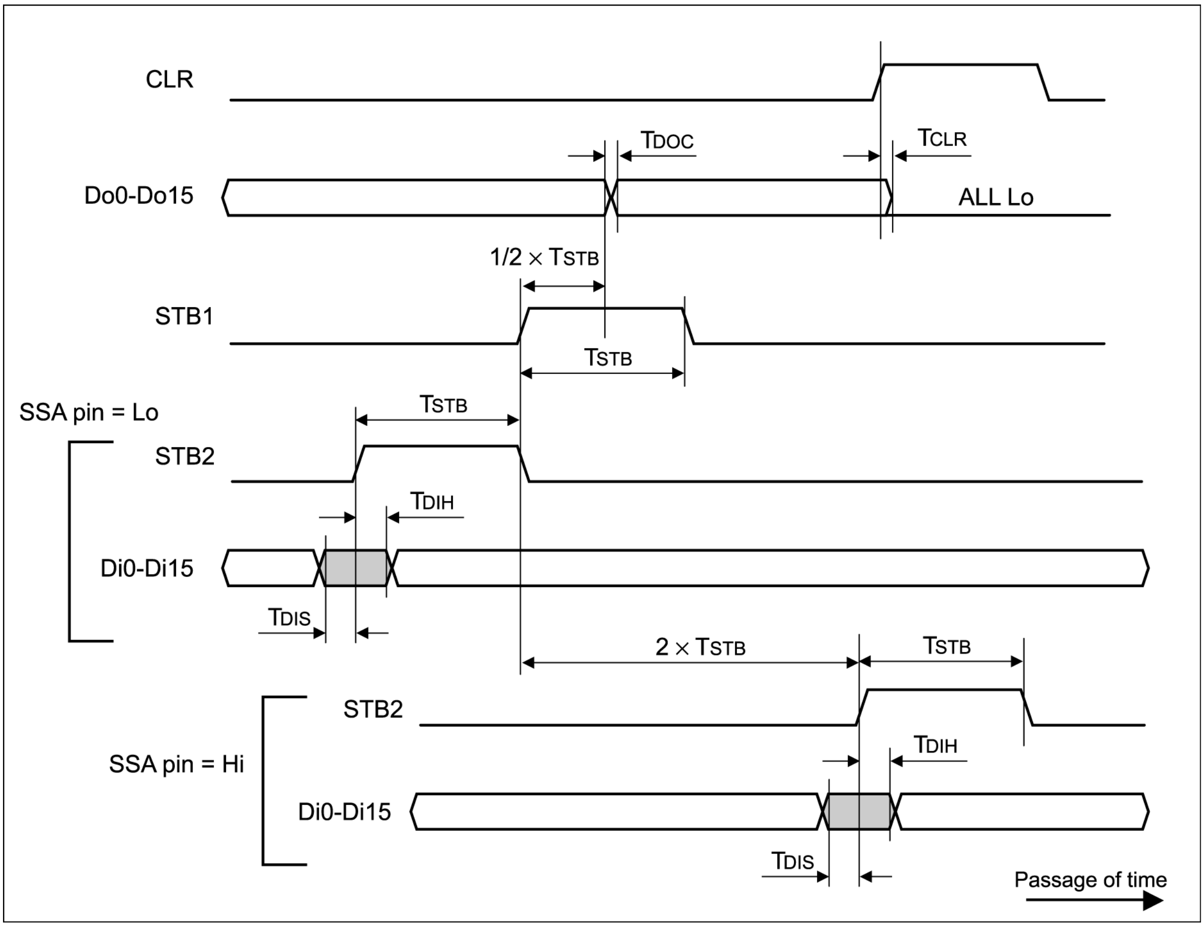
### 5.2.2 Baud Rate Timing (TXE, TXD, RXD)




| Symbol | Baud rate | Short pulse width of sending signal | Unit |
|---|---|---|---|
| TBPS | 12 Mbps (Xi = 48 MHz) | ≈ 83.33 ± 5 | ns |
| | 6 Mbps (Xi = 24 MHz) | ≈ 166.67 ± 5 | ns |
| | 3 Mbps (Xi = 12 MHz) | ≈ 333.33 ± 5 | ns |

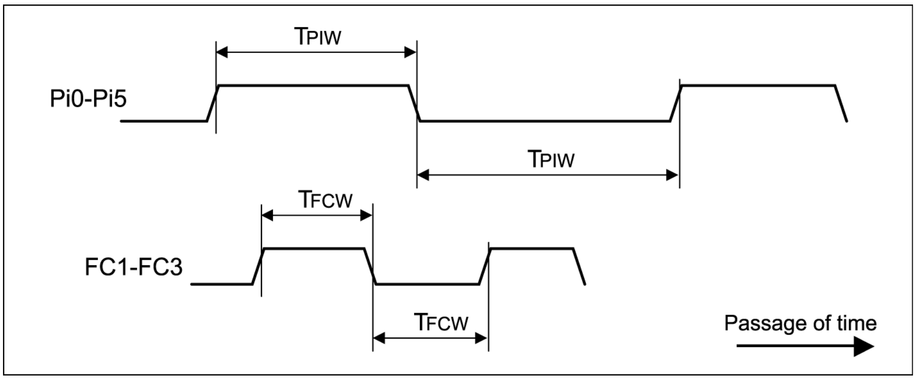
| Symbol | Name | Min. | Typ. | Max. | Remarks |
|---|---|---|---|---|---|
| TTXEH | Period in which TXE pin goes High | (142 × TBPS) - 5ns | 142 × TBPS | (142 × TBPS) + 5ns | -------- |
| TRNW | Short pulse width of input signal | 0.51 × TBPS | 1.0 × TBPS | 1.49 × TBPS | Allowable pulse width as RZ signal |
| TRWW | Long pulse width of input signal | 1.51 × TBPS | 2.0 × TBPS | 2.49 × TBPS | Allowable pulse width as RZ signal |

### 5.2.3 Strobe/I/O Pin Timing (Do0 to Do15, STB1, Di0 to Di15, STB2, CLR)



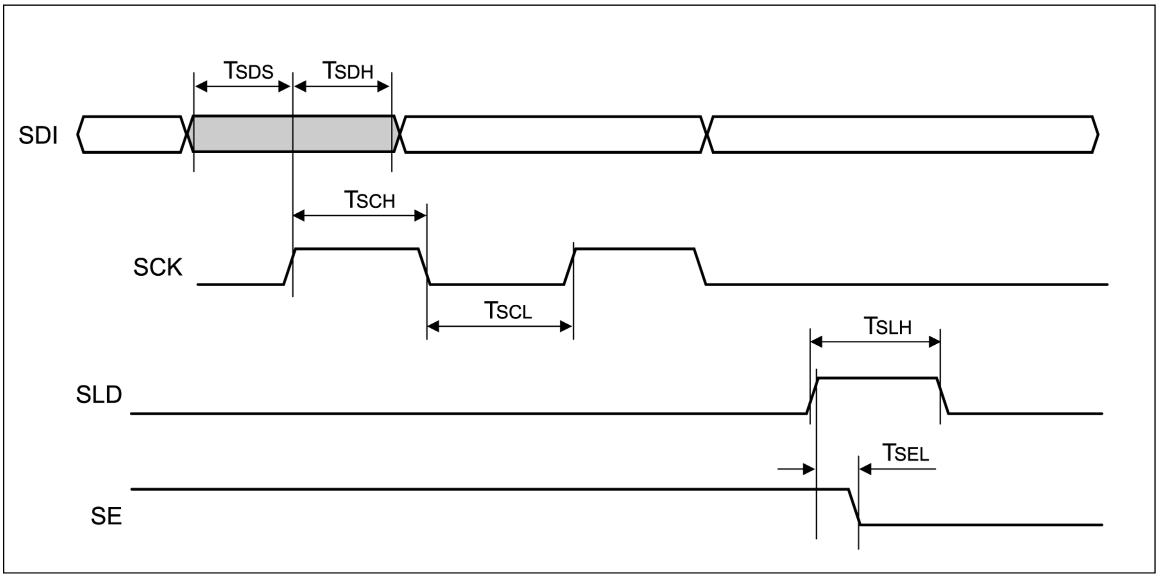

| Symbol | Name | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| TSTB | High-level width of strobe signal | (8 × TXI) - 5 | 8 × TXI | (8 × TXI) + 5 | ns |
| TDOC | Do data transition time | --- | --- | 30 | ns |
| TDIS | Di data setup | 20 | --- | --- | ns |
| TDIH | Di data hold | 0 | --- | --- | ns |
| TCLR | High-level sensing of CLR pin | 3 | --- | 200 | ns |

## 5.2.4 Count Input/Filter Clock Timing (Pi0 to Pi5, FC1 to FC3)



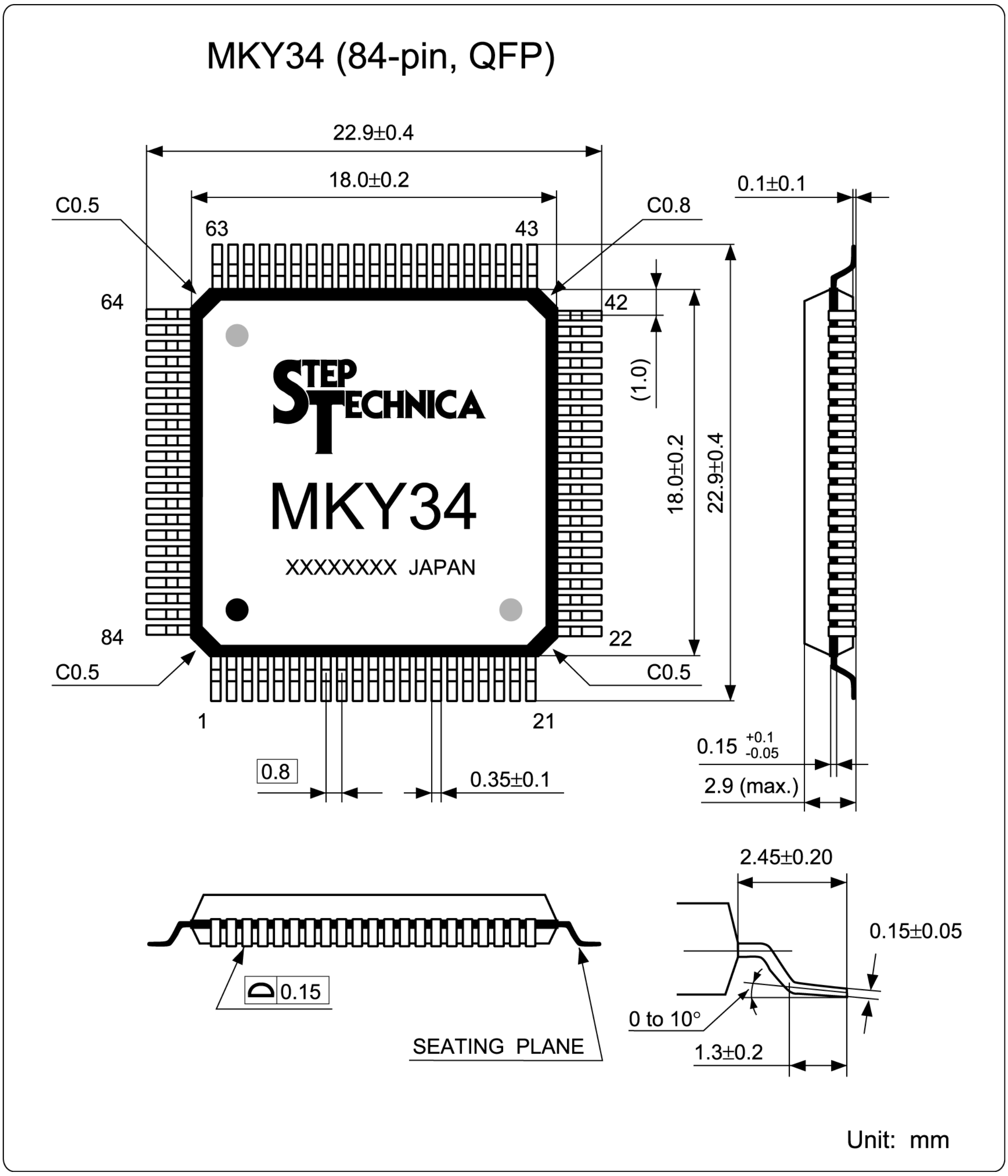

| Symbol | Name | Min. | Max. | Unit | Remarks |
|---|---|---|---|---|---|
| TPIW | Time for keeping count input level | (8 × TXI) + 10 | --- | ns | OAM Pin = Low |
| | | (2 × TFCW) ∩ (8 × TXI) + 10 | --- | ns | OAM Pin = High |
| TFCW | Time for keeping filter clock level | TFCW > TXI | --- | ns | -------- |

## 5.2.5 Input Timing of Serial ID Send Function (SDI, SCK, SLD, SE)




| Symbol | Name | Min. | Max. | Unit |
|---|---|---|---|---|
| TSDS | SDI Setup | 20 | --- | ns |
| TSDH | SDI Hold | 0 | --- | ns |
| TSCH | SCK High level width | 20 | --- | ns |
| TSCL | SCK Low level width | 20 | --- | ns |
| TSLH | SLD High level width | 20 | --- | ns |
| TSEL | SE Response time | --- | 100 | ns |

## 5.3 Package Dimensions



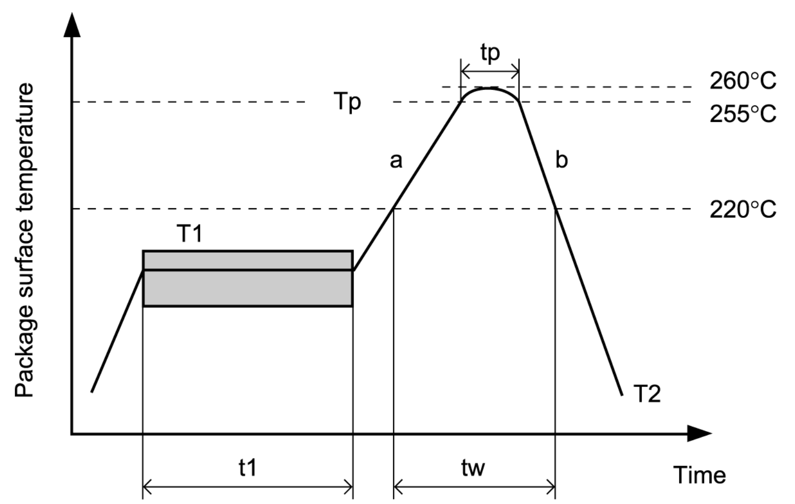
## 5.4 Recommended Soldering Conditions

| Parameter | Symbol | Reflow | Manual soldering iron |
|---|---|---|---|
| Peak temperature (resin surface) | Tp | 260°C max. | 350°C max. |
| Peak temperature holding time | tp | 10 s max. | 3 s max. |

**Caution**

(1) Product storage conditions: TA = 30°C max., RH = 70% for prevention of moisture absorption
(2) Manual soldering: Temperature of the tip of soldering iron 350°C, 3 s max.
(Device lead temperature 270°C, 10 s max.)
(3) Reflow: Twice max.
(4) Flux: Non-chlorine flux (should be cleaned sufficiently)
(5) Ultrasonic cleaning: Depending on frequencies and circuit board shapes, ultrasonic cleaning may cause resonance, affecting lead strength

## 5.5 Recommended Reflow Conditions




| Parameter | Symbol | Value |
|---|---|---|
| Pre-heat (time) | t1 | 60 to 120/s |
| Pre-heat (temperature) | T1 | 150 to 180°C |
| Temperature rise rate | a | 2 to 5°C/s |
| Peak condition (time) | tp | 10 ±3 s max. |
| Peak condition (temperature) | Tp | 255 + 5°C |
| Cooling rate | b | 2 to 5°C/s |
| High temperature area | tw | 220°C, 60 s max. |
| Removal temperature | T2 | ≦ 100°C |

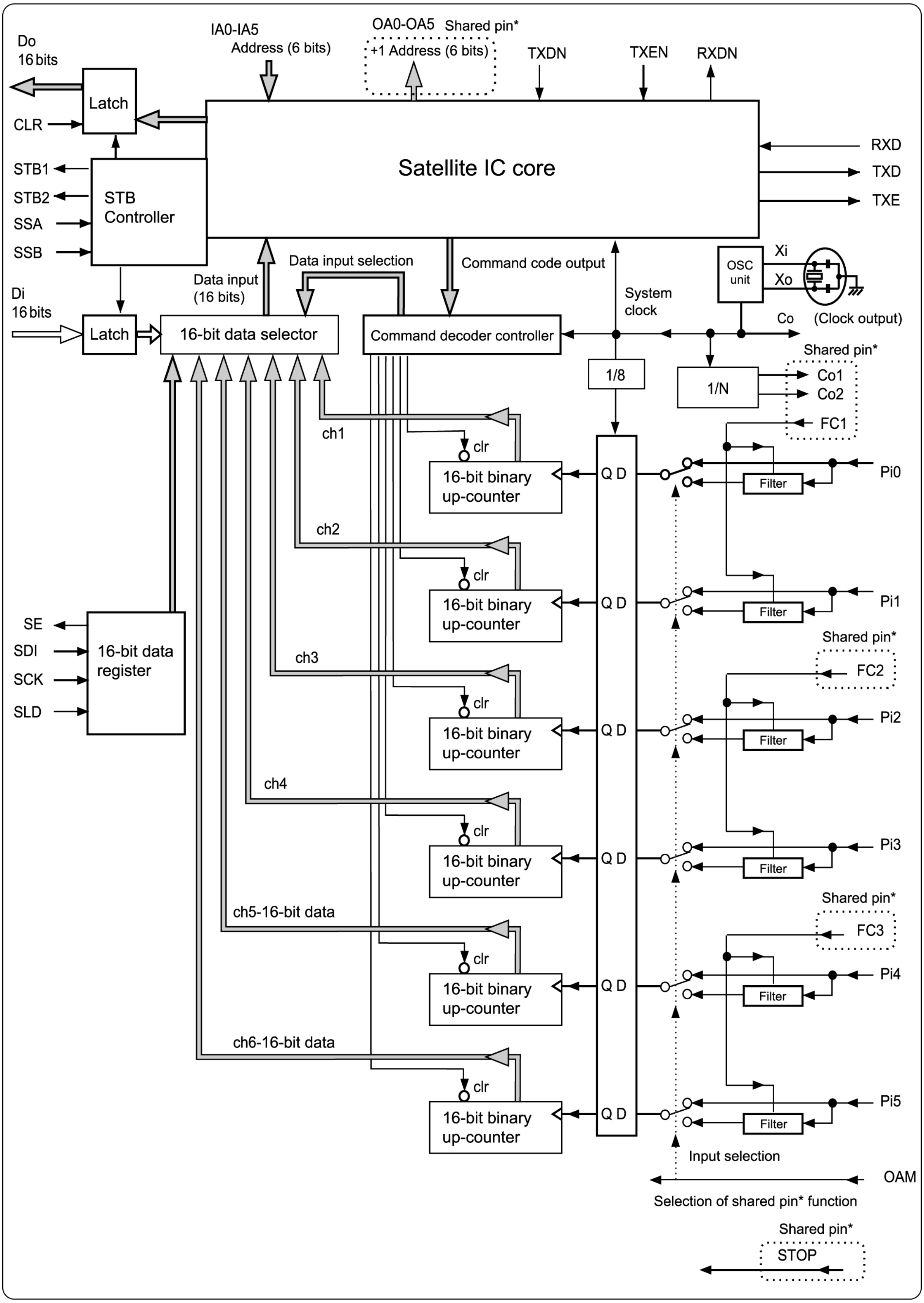
**Caution**

The recommended conditions apply to hot-air reflow or infrared reflow. Temperature indicates resin surface temperature of the package.

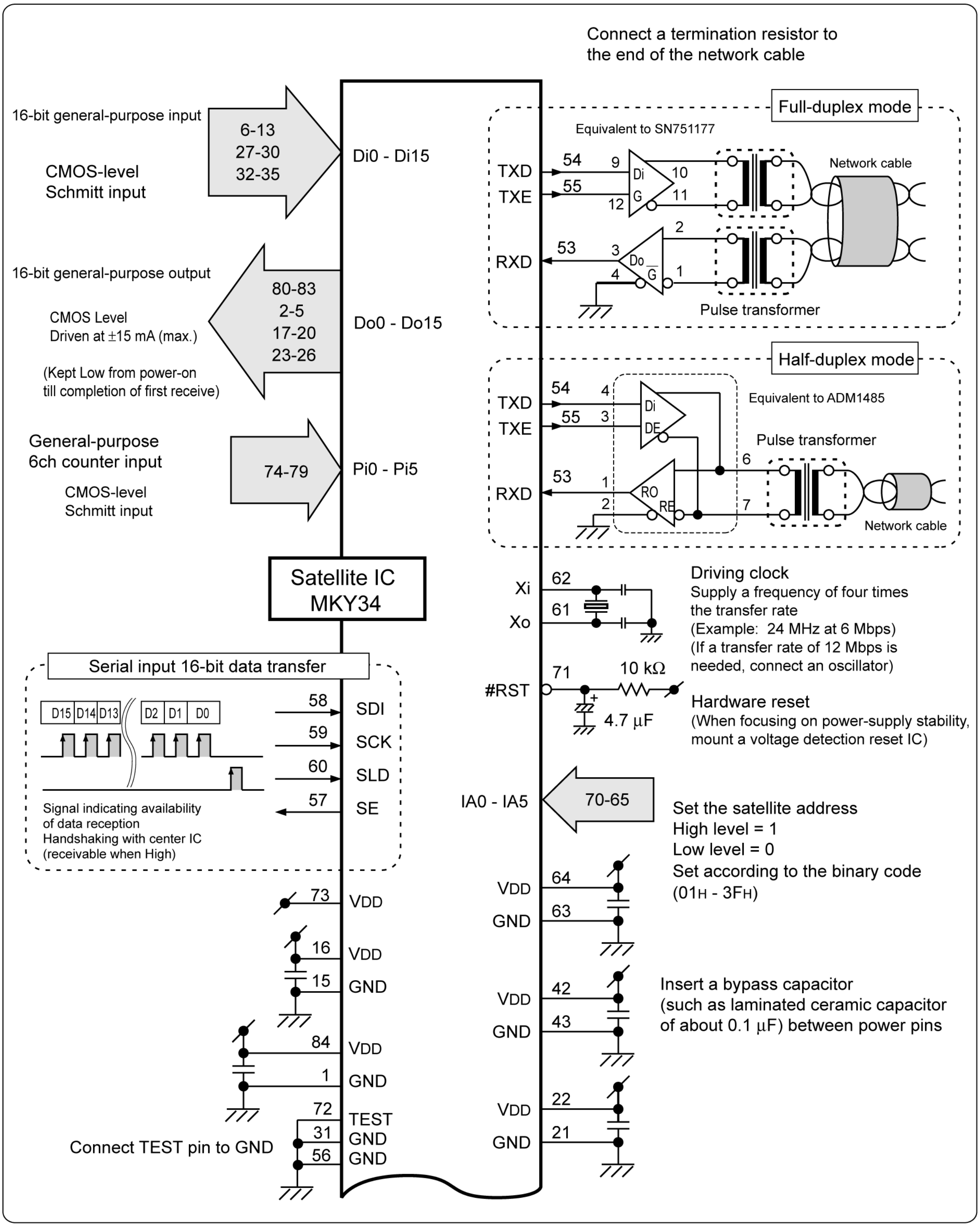
# Appendix

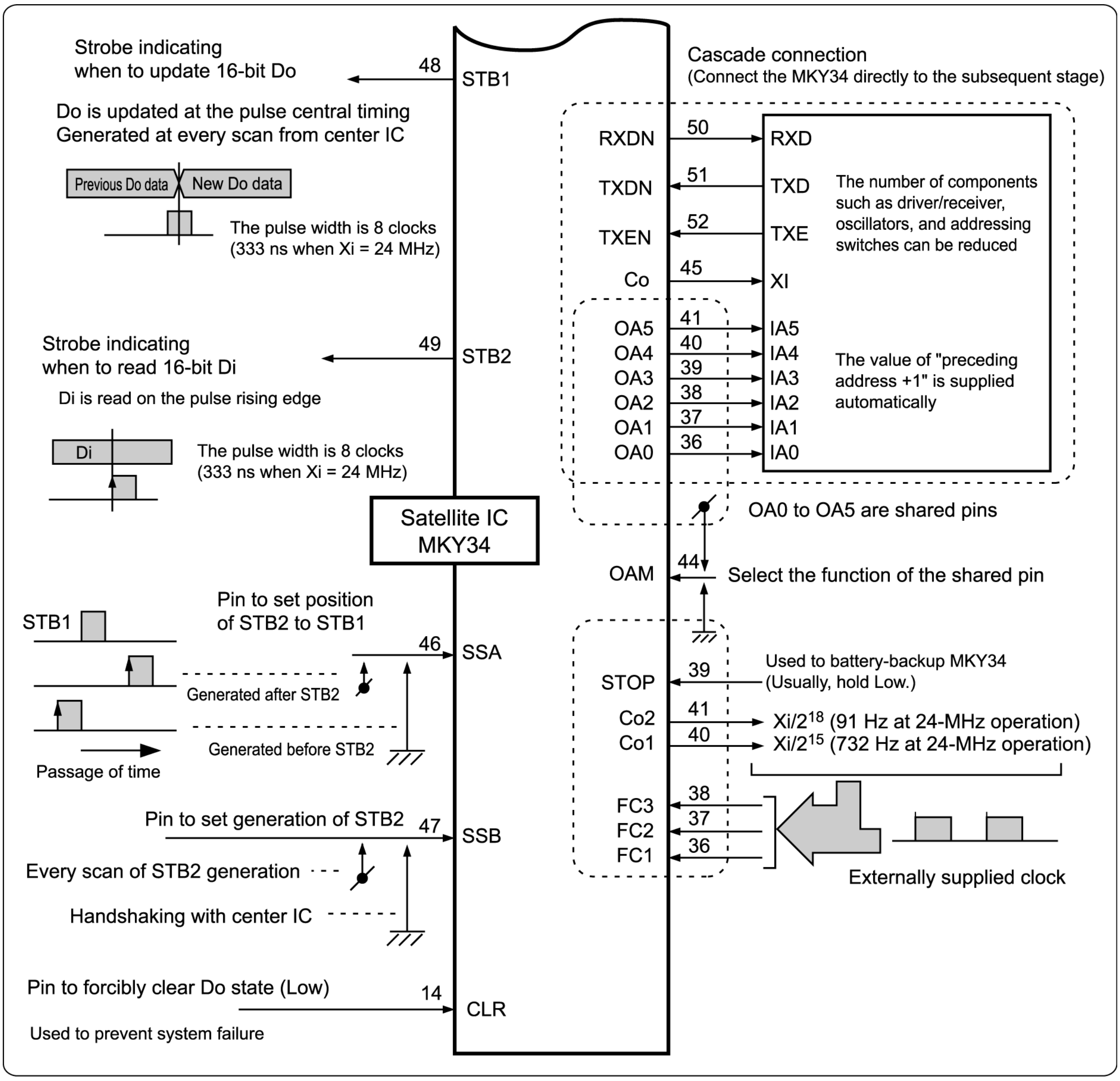
# Appendix

## Appendix 1 Internal Block Diagram of MKY34

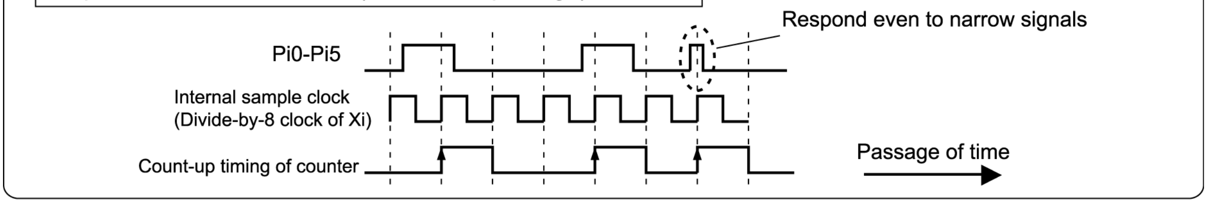


# Appendix 2 Schematic Diagram of MKY34 Function

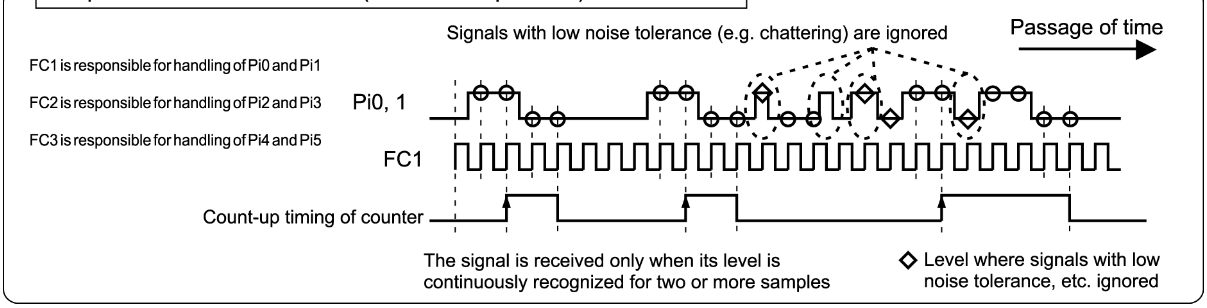





## Operation of 16-bit counter (when OAM pin High)




## Operation of 16-bit counter (when OAM pin Low)



■ North America Distributor

**Trans Data Technologies, Inc.**

340 Arthur Ave.
Roselle, IL 60172
Telephone: 630-440-4075
Facsimile: 630-539-4475

**e-mail: info@steptechnica.us**
**http://www.steptechnica.us/**

■ Developed and manufactured by

StepTechnica Co., Ltd.

757-3, Shimo-fujisawa, Iruma-shi, Saitama
358-0011
TEL: 04-2964-8804
FAX: 04-2964-7653
http://www.steptechnica.com/
info@steptechnica.com

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